# *DESIGN OF 4-BIT MULTIPLEXER USING SUB-THRESHOLD ADIABATIC LOGIC (STAL)*

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*ABSTRACT*

**Objective:** This paper presents the low power consumption for Very Large Scale Integration (VLSI) design. The dynamic power consumption of CMOS circuits is continuously becoming a major concern in VLSI technique. **Tool:** All the simulations in this work are done using Tanner EDA Tools V14.11. **Contribution & Results:** In this paper the 4-Bit STAL multiplexer design have been analyzed and low power multiplexer is designed using the positive feedback logic. The STAL multiplexer is a Positive Feedback-STAL consumes less power than the CMOS multiplexer is identified from this study. **Applications:** In mere future the system can be enhanced to perform higher order bits.

Keywords— CMOS, multiplexer, power consumption, VLSI, STAL, Positive Feedback STAL.

## I. INTRODUCTION

The major objective of this work is to provide an optimal solution for the VLSI low power designers. This work mainly focuses on the minimizing of the total power dissipation, which results in a rapid growth with the scaling down of the technologies. Several techniques at the various levels of the design process have been implemented to reduce the total power dissipation in the circuit, architectural as well as the system level. Additionally, the number of gates per chip area is constantly increasing, while the gate switching of the circuit's total energy does not decrease at the same rate, such results in the rise of power dissipation and heat transfer becomes more complicated and expensive. Then, to curb the power dissipation, a substitute solution at each levels of abstraction is proposed. The dynamic power demand of CMOS circuits is rapidly fetching a crucial concern in the design of distinctive information systems and large computers. In this proposed work, a new CMOS logic family called SUB-THRESHOLD ADIABATIC LOGIC, based on the STAL switching principle is presented for the design of 4-Bit multiplexer. The term STAL originates from thermodynamics, which is used to denote a process in which there is no transfer of heat with the surroundings. The STAL logic structure substantially reduces the power dissipation. The Sub-Threshold Adiabatic switching technique can achieve very low power Dissipation, but at the extortionate of circuit complexity. STAL proffers a way to reuse the energy hoarded in the load capacitors rather than the conventional way of discharging the load capacitors to the ground. Thus, minimum power consumption during charge transfer phase known as STAL switching has been studied from the literatures. Conventional CMOS based designs consume a lot of energy during switching process. STAL switching technique reduces the energy dissipation through PMOS during charging process and reuses the energy stored on the load capacitor during discharging. It consists of two cross-coupled transistors M1 and M2 as load devices and two NMOS transistors in the functional unit. It processes and produce complementary inputs and outputs.

## II. SUB THRESHOLD ADIABATIC LOGIC DESIGN

The STAL is a Positive Feedback Adiabatic Logic (PFAL) structure, which reduces the power dissipation in an overdramatizing manner. The STAL switching scheme is used to achieve low power dissipation, in exorbitant of circuit complexity. STAL logic proffer a path to reuse the energy deposited in the load capacitors preferably the traditional way of discharging the load capacitors to the ground[1]. It should be well known that the fully STAL operation of the circuit is a consummate condition which may be approached linearly as the STAL switching process is reversed down. In most of the cases, the dissipation in energy corresponding with a charge transfer event is usually collected of a STAL component and a non-Sub-Threshold Adiabatic Logic (nSTAL) component. Therefore, reducing all the energy loss to zero is highly impossible, nevertheless of the switching speed. With the STAL switching approach, the circuit energies are perpetuated preferably than dissipated as heat.

Depending on the practical applications and the requirements, this approach can sometimes be used to reduce the power dissipation of the digital systems [2-5]. Like many other STAL logic families, Reversible logic is a dual-rail logic family constructed especially on a pair of cross-coupled inverters that are supplied using a power-clock, other than static DC power supply. The layout of the appraisal logic is what makes reversible logic an ideal family to implement fully reversible STAL logic[6]. This logic is constructed from nMOS devices are connected between the power-clock and the outputs. These nMOS devices take complementary inputs and are constructed to fabricate a low-resistance track between the power-clock and the asserted output. The non-asserted output should be left with a high-impedance track to power-clock, and will be heaved low by the cross-coupled n-type devices. This means that the function is evaluated when there is sufficient differential between the two outputs, but far more importantly means that by using reverse-flowing data, the outputs can be more completely recovered. This should allow losses to be reduced to leakage. [7-9]

## III. DESIGN & IMPLEMENTATION

All the circuits are verified with several input combination and load capacitor, in Tanner EDA Tool V.14.11. Positive Feedback Sub-Threshold Adiabatic Logic (PF-STAL) Logic is a semi STAL approach which tries to increase the charging and discharging

times maintaining the swing levels. It requires presence of dual nature of input (complemented and un-complemented) and creates dual nature for the output. PF-STAL logic shows very positive aspects in addressing the power issues[10-13]. PF-STAL comes in dual rail logic family which requires both the complementary and Un-complimentary inputs for the logic function[14-17] (Refer Figure 1 to 4).

The Logic function (F) and (F bar) are implemented using NMOS networks alongside the two cross coupled inverts as latch known as sense amplifier which drives the two complementary outputs of the circuit. It consists of two PMOS and two NMOS switches which ultimately prevents the output terminals from degradation of logic levels. One of the logic blocks connects the concerned input to the power clock with a low resistance path and on the same time the other function provides a very high resistance in between the power clock and the other concerned output. But the inverter's network provides the second output a conducting path to the ground. In this way one of the two outputs different is pulled up to the power clock and other down to the ground[14-17] (Refer Figure 1 to 4).

### *a. Conventional and Sub-Threshold Adiabatic Logic (STAL) addressing*

In this technique, the energy dissipation of the CN and CCN reversible logic gates are scrutinized for two different logic switching methods. The first, traditional logic switching, is a simulation of the energy dissipateion performance for a range of different input signal rise and fall times (τ). At the faster speed, this rule becomes equivalent to conventional unrestricted step logic transition. However, as the input logic signal speed is slowed, converting to a ramp function, the Sub-Threshold Adiabatic Logic (STAL) switching principle, can be evaluated. Figure 2 shows a typical input to a CCN gate where the input signal transitions are in the form of a linear ramp function and where $V_a$, $V_b$ and $V_c$ are the input voltages on the three input signals A, B and C respectively[18] (Refer Figure 5 to 7).

In this technique, only input signals that have a different final input logic signal change state. $V_a$ keeps its voltage of +2.5V representing a constant binary 1 while $V_c$ keeps its voltage of -2.5V representing a constant binary 0. $V_b$ moves from -2.5 V to +2.5V as a linear ramp versus time. i.e., changing logic state 0→1. The Sub-Threshold Adiabatic Logic (STAL) addressing is yet another switching method that is also used while investigating the performance for energy dissipation of the Controlled Not (CN) and Controlled Controlled Not (CCN) gates[18-19] (Refer Figure 5 to 7).

A set of i/p logic switching waveforms for a and Controlled Not (CN) gate when executing through Sub-Threshold Adiabatic Logic (STAL) addressing. Where $V_a$, $V_b$ and $V_c$ are the input voltages associated with the three inputs A, B and C respectively shown in Figure 3. The input logic switching transition sequence consists of two phases. In the first phase, all input signals move to the midpoint voltage of 0 volts with a controlled rise time / fall (τ) time (see $V_a$, $V_b$, $V_c$, $t_{rise} = t_{fall} = T/2$, for $t < t_{midpoint}$). In the second phase, input signals move either to their new logic state or back to their original logic state (see $V_a$,$V_b$,$V_c$, $t_{rise} = t_{fall} = T/2$, for $t > t_{midpoint}$). $V_b$ moves from –2.5 to +2.5 i.e. changing logic state 0→1. $V_a$ moves from +2.5 to 0 and back to + 2.5 i.e. maintaining logic state 1. $V_c$ moves from – 2.5 to 0 and back to – 2.5 i.e. maintaining logic state 0[18-19] (Refer Figure 5 to 7).

## IV. Results and Discussion on the Basis of Power

We have designed and simulated 4-Bit Multiplexers based on static CMOS and STAL. But this simulation is based on constant load capacitance, constant frequency and constant room temperature[18-19]. But in the real world, multiplexer need to be work on varying parameters and varying conditions. So, now we will observe the effect of varying condition or varying parameters on Static CMOS Multiplexer and Multiplexer based on STAL and observe, why multiplexer based on STAL is better in power savings then Multiplexer based on Static CMOS. The 4- Bit static CMOS Multiplexer and 4- Bit STAL Multiplexer were compared on different varying parameters on the basis of power dissipation across them[18-19] (Refer Figure 5 to 7).

### *i) Average power consumed by 4-Bit Multiplexer designed with static CMOS family and sub threshold adabatic family for different load capacitance values.*

In this section, we have observed the effect of variation in load capacitance over the average power consumed by 4-Bit multiplexer based on Static CMOS and STAL[18-19]. The load capacitance is varied from 10-Ff-190fF with a step size of 20fF and resulting power consumption is observed. The operating temperature is kept constant i.e 24ºC. Input selected are $D_0$=13Mhz, $D_1$=8Mhz and S=25Mhz. The effect of variation of load capacitance over power dissipation is shown in the table 1[18-19] (Refer Figure 5 to 7).

## V. Conclusion

STAL circuits are low power solutions which will soon replace CMOS based logic circuits. From the above results, it is clearly depicted that STAL logic circuits reduce power dissipation with a design size penalty in terms of transistor count. Circuit simulations show that with the help of PFAL, the energy savings can be reached at a significant level. Utilizing the basic PFAL technology basic gates (NAND & NOR) are implemented, verified and analyzed. From the simulations the functionality of the implemented logic gates is found to be satisfactory.

## VI. Future Scope

- The high cost-per-weight of launching computing-related power supplies, solar panels and cooling systems into orbit imposes a demand for STAL power reduction in spacecraft in which these components weigh a significant fraction of total spacecraft weight.
- Realizing 8-Bit, 16-Bit & 32-Bit multiplexers using 4-Bit multiplexer with the help of STAL families.
- STAL circuits needs non-conventional power supply which causes overhead in terms of area hence overall cost is increased. So, design a new sub threshold adiabatic logic family which can be operated by conventional power supply.

- Switching speed of STAL circuit is slow as compare to CMOS logic. So, design a new sub threshold adiabatic family with better switching speed.

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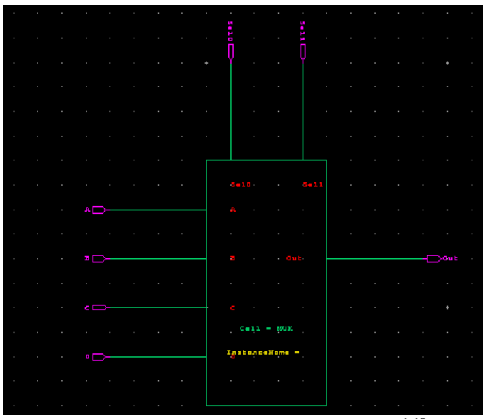

**Figure 1** Block Diagram of STAL multiplexer[1-19]

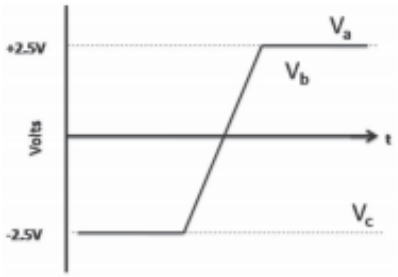


**Figure 2** Conventional switching i/p voltage waveforms of CMOS MUX[1-19]

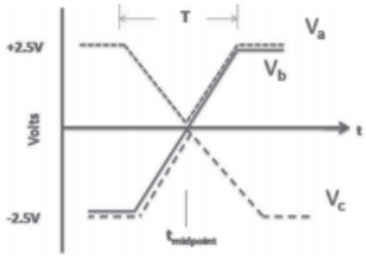


**Figure 3** I/P voltage waveforms for STAL switching in Multiplexers[1-19]

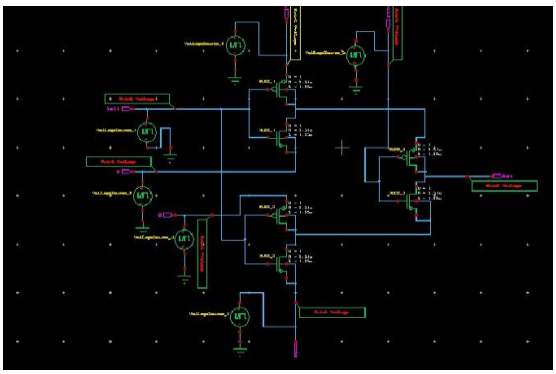

**Figure 4** Circuit of STAL multiplexer

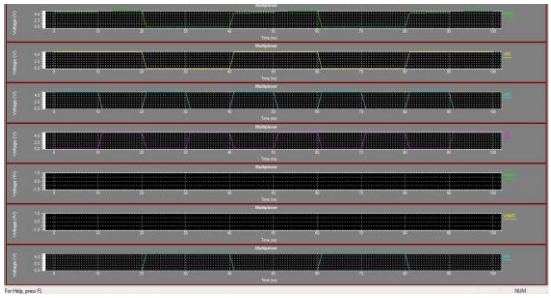

**Figure 5** Output Response of STAL MUX

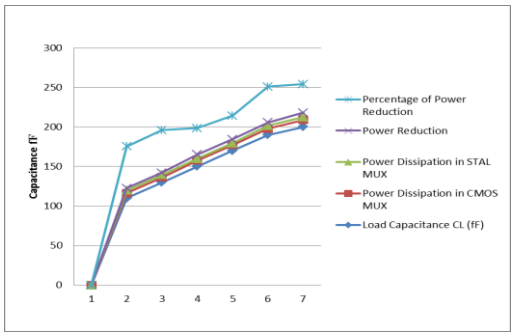


**Figure 6** Performance analysis of power of STAL MUX vs. CMOS MUX

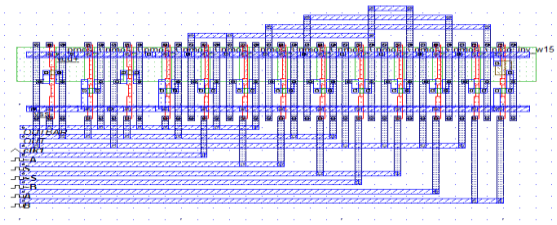

**Figure 7** Layout of 4-Bit STAL MUX

**Table 1** Variation in Power Dissipation with Load Capacitance.

| Load Capacitance $C_L$ (fF) | Power Dissi-pation in CMOS MUX | Power Dissipation in STAL MUX | Power Reduction µw | Percentage of Power Reduction |
|---|---|---|---|---|
| 110 | 6.325 | 3.333 | 2.992 | 52.69 |
| 130 | 6.024 | 3.247 | 2.777 | 53.90 |
| 150 | 7.562 | 2.445 | 5.117 | 33.33 |
| 170 | 7.258 | 2.154 | 5.104 | 29.68 |
| 190 | 7.895 | 3.547 | 4.348 | 44.93 |
| 200 | 8.963 | 3.242 | 5.721 | 36.17 |