ANALYSIS OF AREA DELAY OPTIMIZATION OF IMPROVED SPARSE CHANNEL ADDER

Prajoona Valsalan[1,2] and P. Manimegalai[2]

[2]Karpagam University, Coimbatore, Tamil Nadu, India. [1]Dhofar University, Salalah, Sultanate of Oman, prajoona.v@gmail.com

ABSTRACT

With the revolution in integrated circuits, great emphasis was given on performance and miniaturization. Speed, area and power became the main criterion upon which a VLSI system is measured in terms of its efficiency. In any VLSI system, a full adder is widely component, which decides the performance of the system. The design and analysis of a modified Carry Select Adder(CSLA) is proposed in a cadence 45nm CMOS. It reduces the gate count, thereby area is reduced. Based on modification in CSLA, the process is performed in an efficient way in terms of its gate count and thereby on power and speed.

Keywords: CSLA; Power Consumption; Optimization; AOI; Application-specific integrated circuit; RCA;

1. Introduction

In VLSI industry, the design area and power consumption circuit are rapidly increasing the demand for high-speed systems. In digital circuits, according to the limits of adder speed the propagation of the carry is performed as per the requirement of time. The generating of carry function is performed sequentially as per the carry propagates each bit one after the next. With the indices of a table the address is evaluated.

2.SQRT Carry Select Adder

The Carry Select Adder CSLA) consists of two ripple carry adders (RCA) and a MUX. To add two n- bit numbers, the addition in first RCA is done with Cin=0 and the second RCA with Cin=1. The sum is calculated prior to the correct carry in is known. Once correct Cin is known, then the role of multiplexer comes, which selects the correct sum and carry out is also generated. The number of bits in each carry select block can be uniform or variable. In uniform case, the optimal delay occurs for a block size of √n.

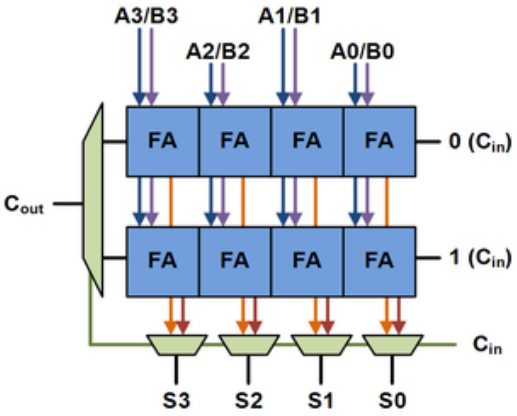

Figure 1. Basic Building Block of CSLA

In digital circuits, the reduction of consumption in a similar speed is process as per the requirement of the data path. In Arithmetic and logic unit (ALU) and digital signal processing (DSP) systems widely used the adder hardware blocks. The computational system of CSLA is used to generate the multiple query function after the sum function. Carry Select Adder (CS-LA) is a faster function of arithmetic in DSP. How-ever, the selection process of RCA multiple pairs is performed by using MUX.

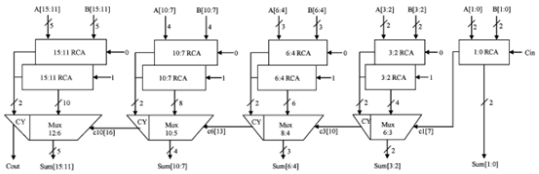

Figure 2. Architecture of CSLA

Each block is grouped as group1, group2 and so on. Since delay of a circuit is the time taken by its longest path of execution and area as number of gates used in it, we can conclude the result as shown in table 1.

Table 1. Delay and area of various circuits

Circuit	Delay	Area
2:1 MUX	3	4
HALF ADDER	3	6
FULL ADDER	6	13

For group 2(2 bit), total number of gates = (No. of full-adders and No. of half adder for Cin=0 calculation) + (No. of fulladders for Cin=1 calculation) + (no. of gates for 6:3 Mux) Total area = 1*6+1*13 + 2* 13 + 12 = 57 Ripple Carry Adder (RCA) is implemented for deriving fast process performances of circuit design, but compared to single RCA design, the number of gates and thereby the area is increased tremendously.

3.Binary to Excess-1 CSLA

Binary to Excess-1 Converter (BEC) [10] is used instead of RCA to achieve consumption reduction in power and area. Both the adders are used for the same purposes, but the performance of BEC is improved than the existing. The general 4-bit circuit of various adders with 8:4 MUX is shown in Figure [3].

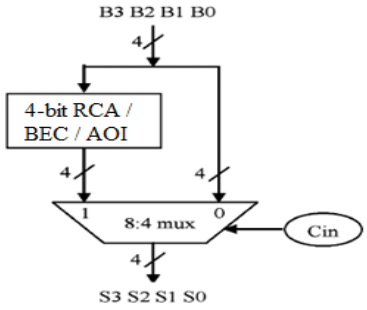

Figure 3. 4-bit Adder circuit with 8:4 MUX

The Binary to Excess- 1 converter (BEC) is designed by replacing the n-bit RCA with Cin=1with (n+1) bit BEC in the SQRT CSLA. The sum and carry from the RCA(Cin=0) is given to BEC. It performs the following function:

X0 = ~ B0, X1 = B0^B1

X2=B2^(B0&B1), X3=B3^(B0&B1&B2) and so on.

In other words, it is equivalent to adding binary 1 to the present input, which is equivalent to action of RCA block with Cin=1.

Figure 4. Function Table of BEC

B[3:0]	X[3:0]
0000	0001
0001	0010
⋮	⋮
1110	1111
1111	0000

The advantage of doing so is that there is no input carry addition in RCA block with Cin=0. So, the n bit adder group, first block in the adder series can be a Half adder and remaining (n-1) Full adders. Therefore, in effect, the gate count is reduced.

For group 2 BEC CSLA, total number of gates = (No. of Half adders) + (No. of Full adders) + (No. of gates to implement BEC) + (Gates to implement 6:3 Mux).

Total area = 1*6 + 1*13 + 2*5 + 2*1 + 12 = 43

So it is clearly evident that the area has reduced considerably by implementing the BEC CSLA compared to conventional SQRT CSLA.

Delay can be calculated for group 2 as the time taken for its longest path of execution ie C3 calculation.

Delay = Delay of (1 HA + 1FA + 1 XOR + MUX)

= 3*1 + 6*1 + 3*1 + 1 = 13

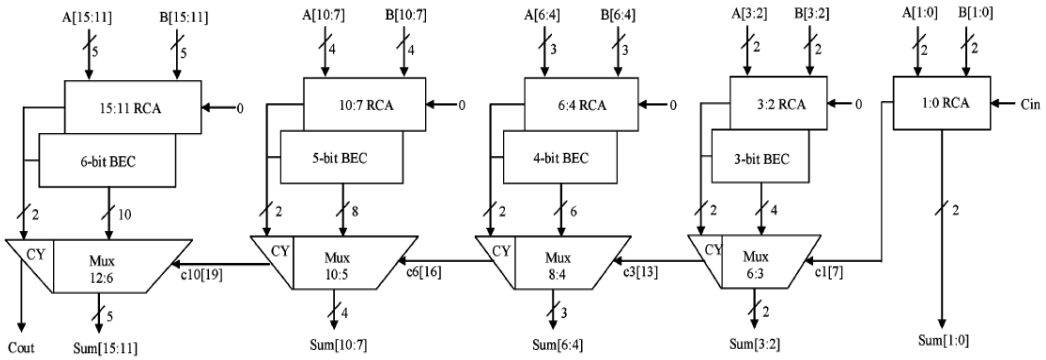

Figure 5. 16-bit BEC CSLA architecture

4.Modified And-Or-Invert SQRT CSLA

The And-Or-Invert CSLA is another alternate way of representing an efficient SQRT CSLA. As discussed in previous section, in BEC CSLA, the second RCA for Cin=1 was replaced by a binary to excess one converter, thereby gate count reduced. In Figure [6], it shows the evaluation of an XOR gate using basic gates And-Or and Not gates, which was considered for all the gate calculations. So, a total of 5 gates were required to implement a single XOR gate.

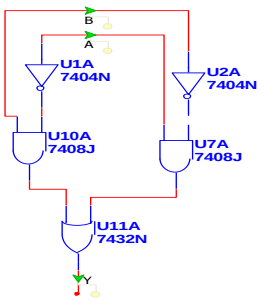

Figure 6. Evaluation of XOR gate for BEC architecture

Another efficient XOR equivalent circuit is designed and shown in the Figure [7]. The XOR gate is designed with only 4 gates with the help of De Morgan's law.

$$\overline{A+B} = \overline{A}.\overline{B}$$

$$\overline{A.B} = \overline{A} + \overline{B}$$

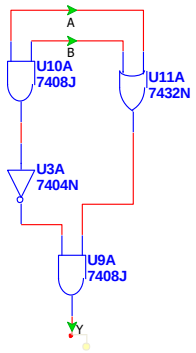

Figure 7. XOR gate for M-AOI architecture

In this proposed design, we replace all the XOR gates in both RCA and AOI with the given circuit. As shown, compared to BEC CSLA, each XOR gate used will have one gate counted less, by implementing the circuit. function performs to have less power, delay and area. The adder blocks perform with low consumption and evaluate it by using the theoretical approach which shows the implementation process effects with area and power. Figure [4] shows the XOR gate implementation in AND, OR and Inverter (AOI). The consuming of the gate generating level and the evaluation of methodology considered the consumption by having 1 unit for each for maximum delay.

The performance of gate operations is done in parallel and indicates the delay for each gates representation. The evaluation of methodology is considered with a maximum delay by the logical block of the gate. By the counting of AOI gates of each block the area evaluation is considered. For better performances of speed and consumption reduction RCA and BEC is replaced with AOI when Cin=1. In modified design, the performances are evaluated by using gate counts than the structure of n-bit Full Adder. For simple and efficient manner, the existing system is modified. Figure [5] shows the replacement of AOI.

In the proposed Modified AOI(M-AOI) design architecture of 64-bit SQRT CSLA is explained in Figure [8]. The existing system modification is shown in Figure [8] with Cin=1. The replacement of AOI is grouped the function of adder in block wise and illustrates the evaluation results of grouped circuit.

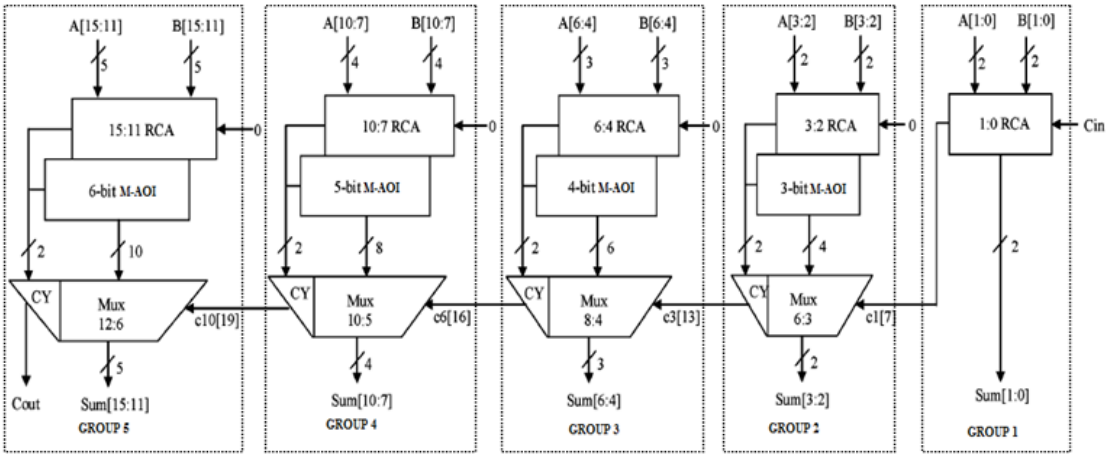

Figure 8. Modified 16-bit SQRT CSLA.

In group 1, only RCA adder is used but in other groups RCA and Modified AOI are used. As similar to group 1 the process function is done with both the adder but here the input is taken from the previous output. The logic modified AOI is replaced in the position of RCA, BEC and AOI when Cin=1. The input selection is considered by the timely arrival and delay. The pervious sum of RCA and AOI is given as input to the next group and the MUX output is computed respectively with the adder. The multiplexer design implementation is coded from 6:3 to 24:11. By using gates the design code is performed on the circuit. The evaluation of the proposed method is implemented in the modified area efficient of 16-bit SQRT CSLA. So the delay doesn't change for the circuits, but the gate count reduces, thereby area is reduced and also the power dissipation.

Table 2. Delay and Area for M-AOI

Circuit	Delay	Area
Half Adder	3	5
Full Adder	6	11

To calculate the total gate count in group 2, one half and full adder (2-bit RCA) is considered with Cin=0. If Cin=1 then 3bit AOI is used and includes one output. The gate count is obtained for group 2 as follows:

For Group 2:

Total number of gates = (No. of Full adders) + (No. Of Half adders) + Number of basic gates AND, OR and NOT gates+ No. of MUX

Area = 1*11 + 1*5 + 4*1+ 2*1 + 3*1 +12*1= 37

5.Implementation

In this section, the circuit design flow and implementation of kit design is explanation and the design is done using Cadence 45nm CMOS process technology. The common Boolean logical terms are shared with the operation of modified AOI gates. The logic gates determine the perform time of the structure with the present input in the combinational circuit. As well as the signal state of logic selection is done through the multiplexer. Therefore, the proposed design performed with less delay, area and power than the existing.

The group structure of the proposed circuit is designed and implemented for the performance improvement of the system. The modifications of the proposed circuit consider the gate replacement. As per the design logic, the hierarchical process proceeds with the specification of logic circuit and also the complete circuit determine the functions by the Carry look ahead network, pre-and post-processing. Figure [8] shows the modified AOI Circuit. The proposed M-AOI circuit is implemented in the groups. Figure [8] shows the modified adder of CSLA (MA-CSLA) with all groups. The proposed structure of group 2 and all groups is shown in Figure [9] and Figure [10] respectively.

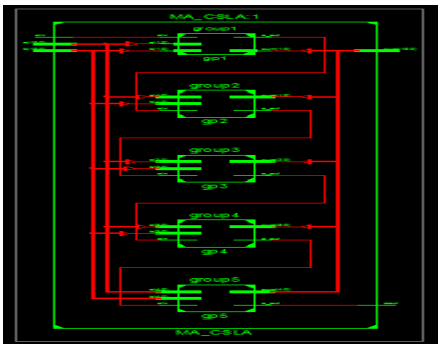

Figure 9. Schematic Diagram - Proposed Circuit

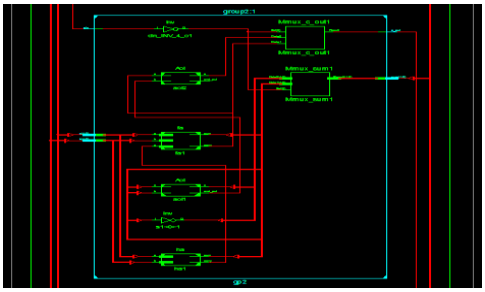

Figure 10. Proposed Circuit of Group 2

6.Simulation Results

The analysis of proposed circuit simulation results is explained and illustrated in this section. The simulation process specification is Power (460uW), Max frequency (374.94MHz) and Area (440µm X 300µm = 0.132 mm^2). The common inputs of CMOS for the process are randomly generated by the CMOS inverter. The layout of the proposed design circuit is done using Cadence Virtuoso Layout Editor Tool. The RTL diagram of the proposed circuit of adder is simulated and analysis as shown in Figure [15]. The simulation of BEC architecture and M-AOI is shown if Figure [11] to Figure [14].

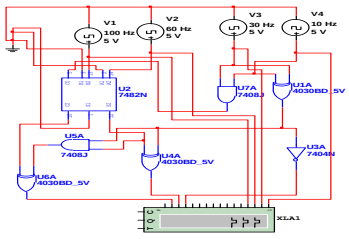

Figure 11. Simulation circuit for BEC architecture

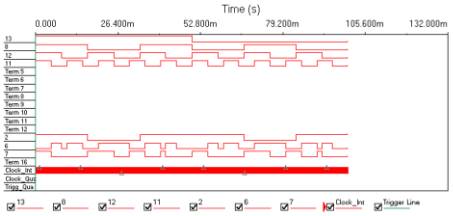

Figure 12. Simulation output for BEC

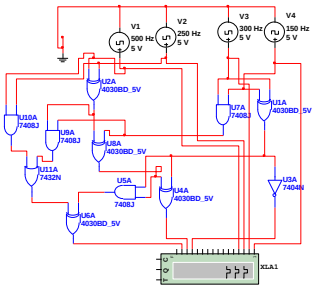

Figure 13. Simulation circuit for M-AOI architecture

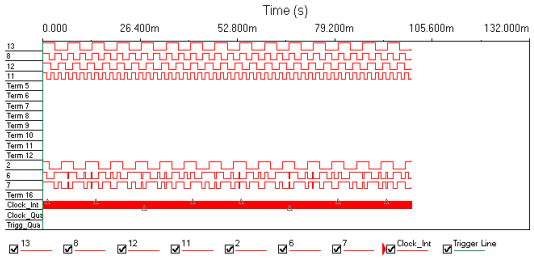

Figure 14. Simulation output for M-AOI

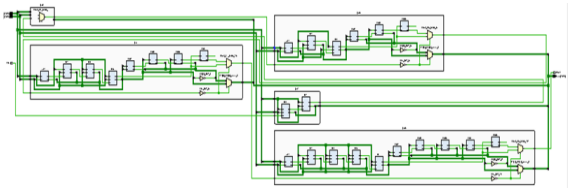

Figure.15. RTL Schematic Diagram of Proposed Circuit

Table 3. Performances analysis of adder circuits

Adder (Word Size 8 Bit)	Area (gate count)	Delay (ns)	Power (mW)	Power Delay Product (pWs)
Regular SQRT (Dual RCA)	132	10.98	182	2300.56
Modified QRT (with BEC)	128	12.25	175	2464.2
Modified SQRT (with M-AOI)	105	10.82	151	1633.82

7.Conclusion

In VLSI design, factors which are essential for a circuit ie area, delay and power analysis is performed. In this proposed circuit, it is designed in order to overcome the disadvantages of the various existing circuits. The Modified 16-bit SQRT CSLA is proposed for the improvement of performances in gate count reduction, less delay and lower power than the existing. Also provides faster process and provide implementation in a simple and easy manner. In VLSI, the proposed hardware implementation is performed in an efficient access by simulating the circuit using the library function of gpdk in a Cadence 45nm CMOS process and Multisim. The proposed modified SQRT CSLA analysis shows that power and delay is improved, therefore making the design efficient. Future work aims to test the proposed design by using three input XOR gates and to improve the performances of parameter level.

8.References

[1] B. Anand, Teresa V.V., An Improved Low power and Modified Area Efficient Carry Select Adder (MA-CSLA). International Journal of Applied Engineering Research (IJAER) (2014)

[2] Garima Singh, Design of Low Area and Low Power Modified 32-BIT Square Root Carry Select Adder. International Journal of Engineering Research and General Science 2(4): (2014)

[3] ShuchiVerma, Sampath Kumar V., Design & Analysis of Low Power, Area-Efficient Carry Select Adder. Int. Journal of Engineering Research and Applications 4(3): Version 1, 53-56 (2014).

[4] K.Saranya, Low Power and Area-Efficient Carry Select Adder. International Journal of Soft Computing and Engineering 2(6): (2013)

[5] Veena V Nair, Modified Low-Power and Area-Efficient Carry Select Adder using D-Latch. International Journal of Engineering Science and Innovative Technology 2(4): (2013).

[6] PallaviSaxena, UrvashiPurohit, Priyanka Joshi, Analysis of Low Power, Area- Efficient and High Speed Fast Adder. International Journal of Advanced Research in Computer and Communication Engineering 2(9): (2013).

[7] Jayanthi, A.N., Ravichandran, C.S., Comparison of performance of high speed VLSI adders, Current Trends in Engineering and Technology (ICCTET), International Conference Pp.99-104 (2013)

[8] B. Ramkumar and Harish M Kittur, Low-Power and Area-Efficient Carry Select Adder. IEEE Transactions on Very Large-Scale Integration (vlsi) Systems 20(2): (2012).

[9] Deepthi Obul Reddy, P. Ramesh Yadav, Carry Select Adder with Low Power and Area Efficiency. International Journal of Engineering Research and Development 3(3): 29-35 (2012).

[10] B. Ramkumar, H.M. Kittur and P. M. Kannan, ASIC implementation of modified faster carry save adder. Eur.J. Sci.Res. 42(1): 53–58 (2010).

[11] U Ko, P T Balsara and W Lee, Low--power design techniques for high-performance CMOS adders. IEEE Transactions On Very Large Scale Integration System 3(2): 327–333 (1995).

[12] N. Weste and D. Harris, CMOS VLSI Designs, Pearson Wesley (2005).

[13] S. Goel, S. Gollamudi, A. Kumar and M. Bayoumi, On the design of low-energy hybrid CMOS 1-bit full adder cells, Proceedings of the 47th IEEE International Midwest Sympo-sium on Circuits and Systems Pp. 209-212 (2004).

[14] Y. Jiang, A. Al-Sheraidah, Y. Wang, E. shah, and J. Chung, A novel multiplexer-based low power full adder. IEEE Transaction on Circuits and Systems 51(7): 345-348 (2004).

[15] Kuldeep Rawat, Tarek Darwish and Magdy Bayoumi, A low power and reduced area Carry Select Adder, 45th Midwest Symposium on Circuits and Systems 1: 467-470 (2002).

[16] D. Radhakrishnan, Low-voltage low-power CMOS Full Adder, IEE Proceedings: Circuits, Devices and Systems 148(1): 19–24 (2001).

[17] Y. Kim and L.-S. Kim, 64-bit carry-select adder with reduced area. Electron. Lett. 37(10): 614-615 (2001).