DESIGN OF LOW INTRICATE 10-BIT CURRENT STEERING DIGITAL TO ANALOG CONVERTER CIRCUITRY USING FULL SWING GDI

Keerthivasan S., Mahendra Babu G.R., Rajendran T.

Department of ECE, FOE-CB, Karpagam Academy of Higher Education (Deemed to be University), Coimbatore, India. keerthivasan1608@gmail.com, arajrajesh1990@gmail.com

ABSTRACT

Aim / Objective: A low-vigor, low-voltage, small- area DAC for prime pace applications is introduced on this paper, for top velocity purposes, the present steering DAC is also used because the entire currents taken from the supply is utilized for the output signal. **Scope:** This paper it deals with the design and evaluation of a 10-bit FS-GDI DAC which was once applied making use of full Swing (FS) GDI logic in CMOS system. **Results:** The lively subject of this proposed DAC was decreased to four times in a normal 0.18 µm with a varying voltage variety from 2.5 – 3.3V CMOS approach, each the INL and DNL have been decreased for the proposed scheme of 10-bit FS-GDI DAC, although it's a procedure of excessive order utilizing FS-GDI DAC. **Applications:** Utilized for high speed processing circuitries.

Keywords: DAC, CMOS, FS-GDI Logic, INL & DNL

I. INTRODUCTION

In past various decades, the present controlling converter is being burdens perceived hardware for its radical speed Digital to Analog Converters. The present steerage DACs are well-near presumably the most powerful and vigorous structure to technique the determination beneath 10 bits and likely basically the most needed. The proposed current-directing outline of a DAC[1] as shown in Fig.1 can instantly connect heap imperviousness to the voltage inside the yield stage, inside the nonattendance of a present enhancer[1]. There is zero capacitance inside the circuit, and there is no requirement for charging and releasing of current while at activity[2]. The fundamental hindrances are its affectability to gadget jumble; provisional technique imperfections and the yield impedance of prize give are higher to immense number of bits.

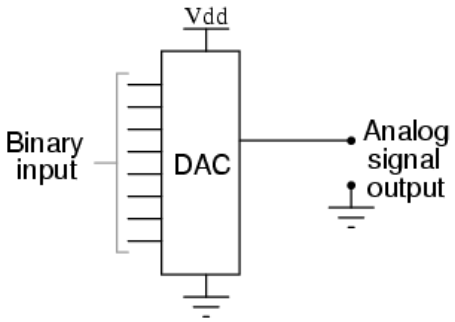

Fig. 1 Simple DAC

A self-adjusted circuit may even be intended to cure these difficulties; however, the hardware will eat up additional power and require a colossal field. CS-DACs are pertinent for high choice outline and unnecessary %. The utilized current-steerage models are Thermometer constitution, Binary weighted and portioned designs. The Thermometeric structure[3] can likewise be referred to as a unary weighted constitution, which has stood out measurement reward supply. An N-bit thermometer DAC requires 2N−1 homogeneous present sources to incite 0–2N−1 voltage develop. At the point when a switch prompts, the yield cost raises with the guide of one Least monster Bit (LSB). The thermometric constitution of present steerage Digital to Analog Converter is monotonic, proposes simply remedy linearity and minimizes the size of procedure deformities given that it switches stand out transistor switch over the span of single clock. The unary weighted DACs persevere from structure difficulty, a huge chip teach and power utilization. In this way, they don't appear to be good for high determination DAC circuit outline. Parallel weighted structure constitution is characterized in[4, 5] which may be exceptionally helpful and requires insignificant control and negligible life utilization, as it's going to most likely quickly utilize the double information code to snatch the exchanging of current sources, with none interpreting standard sense request[6]. The primary circumstance of double weighted structure is degraded execution in view of framework shortcomings, prevalently at focus code moves and complex current supply coordinating necessities. For e.g., a 4bit paired info code shift 0111 directly into a thousand, which get to excessively numerous present sources in a solitary title and deliver huge adequacy system imperfections, which create more life utilization. Sectioned structure[7] is a mixture of thermometric and paired weighted structure.

MSB pieces use thermometric example for bigger exactness, and LSB squares utilize the plan of twofold weighted, such divided structure diminishes the intricacy in order and power utilization of the D-A converter. The Least gigantic Bit (LSB) actuates little plentifulness framework imperfections as background noise the recurrence zone[6]. An excessive number of portioned stages can amplify the computerized clamor and worsen the effectiveness [8]. The static effectivity of DACs reminiscent of DNL and INL must be considered, also because the dynamic execution of DACs likes SFDR. A DNL should be littler than 1 LSB, and the Digital to Analog converter will must be spared monotonic. Every advancement inside the computerized info code raises the simple yield charge. The DNL is always littler than 1 LSB if the INL is littler than 0.5 LSB. A crucial INL must be not up to 0.5 LSB, which guarantees that the great linearity mistake is littler than the most extreme quantization blunder[9]. Fig. 2 portrays a theoretical of the DAC structure.

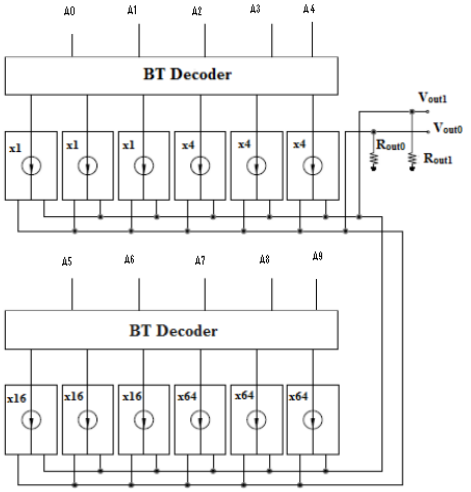

Fig. 2 Simple DAC Architecture.[9, 10]

II. DIGITAL TO ANALOG CONVERTER ARCHITECTURE: The DAC circuit comprises both BT (binary to Thermometric) modules known as BT decoder9, 10 and current source modules (includes of both present reflect and a switching circuit) as shown in fig. 2 9, 10. The 10-bit Digital to Analog Converters (DAC) module involves two BT decoders, as shown in Fig.1. The first BT decoder transfers A7–A4 to thermometric code, which has the authority of on/off of 64-I0 and sixteen-I0 present source[9, 10]. The 2nd BT decoders switch A3–A0 to thermometric codes, which controls the on/off of four-I0 and 1-I0 present source, respectively[9, 10].

III. BINARY TO THERMOMETRIC DECODER

Fig. 2 demonstrates the 10-bit FS-GDI BT decoder. It comprises of four AND and four OR gates. S0-S17 is the present source's control signals. The 10-bit DAC decoder requires five AND doors and five OR entryways as it were. The Binary to Thermometric (BT) is utilized to change paired code (I9, I8, I7, I6, I5, I4, I3, I2, I1& I0) 2 to 4 thermometric codes (S11, S10 & S9) thermometric, (S12, S13 & S14) thermometric, (S8, S7& S65) thermometric, (S5, S4 & S3) thermometric and (S2, S1 & S0) thermometric as appeared in Fig. 2. The yield current of the present sources controlled by (S11, S10 & S9) thermometric is 4, 16, 64 times of the present sources controlled by (S8, S7& S6) thermometric, (S5, S4& S3) thermometric, (S2, S1 & S0) thermometric individually[9, 10]. This DAC utilizes a BT module as another option to the conventional system, which has focal points than the current complex circuits[9, 10]. A BT decoder contains one AND door and one OR entryway for its legitimate operation. The BT in the DAC Circuitry diminishes the circuit complexity, postpone and control usage separately. Every one of these doors is actualized utilizing CMOS rationale. Six transistors are utilized to play out a rationale operation [9, 10].

The AND, OR gates are applied using FS-GDI logic[9, 10, 11, 12] to lessen the whole quantity of transistors and the total chip discipline. The basic GDI includes two transistors as shown in Fig. 3 & 4. Which contrivance disparate Boolean capabilities as listed in Table I.

Table I Input Configuration of a Simple GDI Cell[9, 10]

N	P	G	OUTPUT	FUNCTION
0	B	A	$\bar{A}B$	F1
B	1	A	$\bar{A}$+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	$\bar{A}$B+AC	MUX
0	1	A	$\bar{A}$	NOT

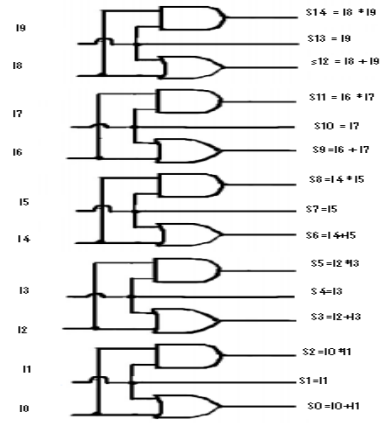

Fig. 3 FS-GDI 10-Bit BT Decoder[9, 10]

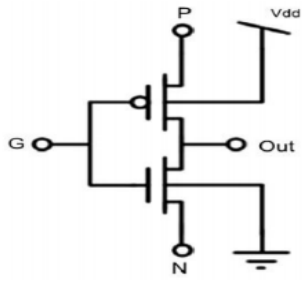

Fig. 4 A Simple GDI Cell[9, 10]

The drawbacks of GDI logic gates are overcomes by initiating FS-GDI Logic gate, which are figured in Fig. 5. & Fig.6. [9, 10, 11, 12]

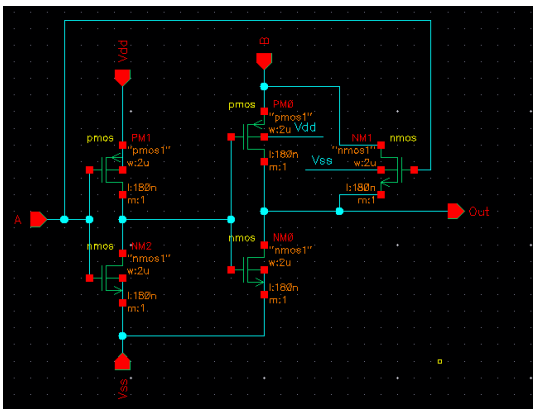

Fig. 5 Circuit of FS-GDI AND gate. [9, 10, 11, 12]

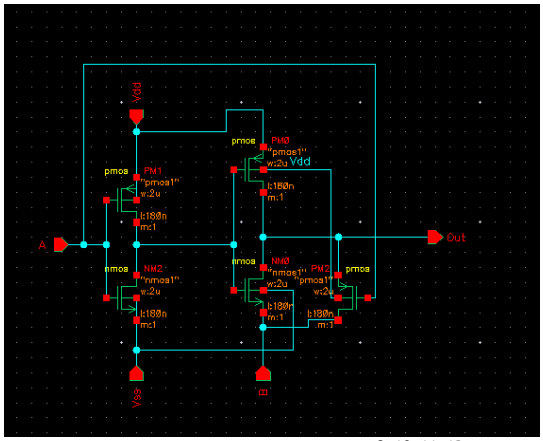

Fig. 6 Circuit of FS-GDI OR gate. [9, 10, 11, 12]

IV. CURRENT SOURCE MODULE

The present source in the proposed DAC is figured in Fig. 7. The MOS transistor p_1 operates within the saturation neighborhood and controls the worth of the present in each present supply. The current readings of the 10 current sources can be calibrated with the aid of altering the width of MOS transistor p_1[9, 10, 11, 12]. The bias voltages Vin and V_{in1} are additionally first-rate-tuned in this sort of means that MOS transistors p_1, p_2 and p_3 can function within the saturation vicinity. MOS transistor p_3 is used to make stronger the output impedance of the circuitry. The high output impedance can strengthen the performance of INL and SFDR[9, 10, 11, 12].

The perfect intention of the MOS transistors SW_0 and SW_1 are to participate in the process of switching. The gate signal of SW_0 is hooked up from the BT decoder output, i.e., Thermometric code (S2, S1 & S0)[9, 10, 11, 12]. As Si = 1, where 0≤i≤2, MOS transistor SW0 turns on the change and MOS transistor SW_1 turns it off. The Current sources (CS) are grown to become on and the current flows by means of the output resistor Rout0 to generate an analog output signals from the Digital to Analog Converter. As MOS transistor SW1 turns on, MOS transistor SW_0 turns off, and the current trickle along the output resistor Rout1 to generate an inverse sign, that is for a single present source module 9, 10, 11, 12.

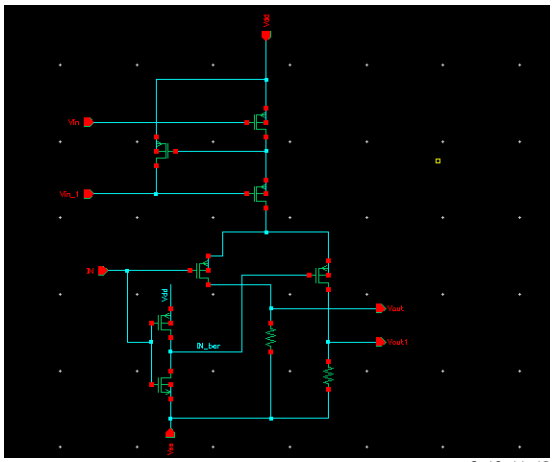

Fig. 7 Circuit of FS-GDI Current source module[9, 10, 11, 12]

The 10-Bit FS-GDI (in Fig.8.) requires 12 CS's and the entire currents from each current source are summated on the output stage. The output voltage and currents are given by the following equation (bench marked from[9, 10, 11, 12])

$$V_{out} = I_{out} * R_{out}$$

$$I_{out} = [(B1 \vee B0)+(B1)+(B1 \wedge B0)](1_{unit})$$
$$+[(B3 \vee B2)+(B3)+(B3 \wedge B2)](4I_{unit})$$
$$+[(B5 \vee B4)+(B5)+(B5 \wedge B4)](16I_{unit})$$
$$+[(B7 \vee B6)+(B7)+(B7 \wedge B6)](64I_{unit}).$$

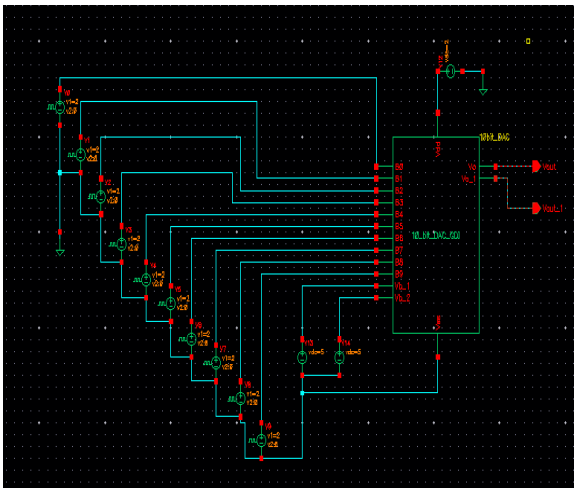

Fig. 8 Schematic of 10-bit DAC using FS-GDI logic.

Here, V_{out} is an analog output voltage, I_{out} is total current utilized by all the current sources and Rout is output resistance. This 10- bit FS-GDI DAC output can provoke a differential analog signal at the output stage. [9, 10, 11, 12]

V. METHODOLOGY

[13-15]FS-GDI procedure was offered as a positive replacement to complementary CMOS logic design and GDI common sense. The scheme was at the start proposed for fabrication in SOI and twin-good CMOS processes. The FS-GDI system makes it possible for enactment of a broad variety of complex logic services making use of two transistors. It is delivered that subject and dynamic power of FS-GDI combinatorial and sequential good judgment have been remarkably minimized, as in comparison with CMOS schemes and GDI schemes. The place its, one of the most inputs are undeviatingly dispersed into the gates of the MOS transistors of N-style and P-style. Gate Diffusion enter scheme minimizes the energy dissipation, swing prolong, and the chip subject.

- ✓ Full Swing Gate Diffusion input (FS-GDI telephone) comprises three inputs they are G-(normal gate enter of NMOS transistor and PMOS transistor), P-(enter to the source or drain of PMOS transistor), and N-(enter to the supply or drain of NMOS transistor)[13-15].
- ✓ The source of PMOS transistor in a FS-GDI phone just isn't bridged to VDD and source of NMOS transistor is just not bridged to GND. This selection offers FS-GDI phone two additional input pins for use which makes FS-GDI technique extra nontoxic[13-15].
- ✓ Bulks of both NMOS transistor and PMOS transistor are linked to N or P (in my opinion), so it is going to be whimsically biased in a assorted with CMOS inverter circuitry[13-15].

An easy change in the input configuration of the simple FS-GDI phone corresponds to a drastic alternate in the Boolean functions. Most of these functions require countless gates in CMOS, nevertheless it's very simple in the FS-GDI design techniques. GDI makes it possible for easier gates, reduce transistor depend, and scale back power dissipation. The FS-GDI design provides a original logical building block that can allow complicated capabilities via cognizance utilizing fewer add-ons than current ways[13-15].

The execution and implementation may be very simple, has smaller die size and no more exorbitant solutions. The technology is designed based on common CMOS fabrication and will also be simulated via cadence design instruments. Our design general mobile has only two MOS transistors with 4 terminals: and the three inputs are the fashioned gate and source or drain of every MOS transistor, and an output. With this design configuration, we can understand all ordinary CMOS logic gates – with minimum number of components. Several solutions like MUX are achieved and carried out in a single stage. Using outstandingly reduced complete components utilizes smaller die measurement or area and lesser power.

VI. RESULTS AND DISCUSSION

Fig.8 indicates the 10bit FS-GDI DAC, which contains present source modules of one-of-a-kind weights. The digital enter bits B0 and B1 are drives the primary three current sources of having identical weight and gives a present I0. The present sources driven through inputs B2 & B3, B4 & B5, B6 & B7 are having weights 4, 16 and 64 instances of the present sources driven through B0 & B1 respectively.

The output waveforms of the above 10-bit DAC proven in Fig.9., Fig.10. and Fig.11. Respectively. The full-scale voltage of the DAC divided into equal components and output is a staircase wave which raises one step in output to corresponding to at least one-bit increment in input. The proposed 10-bit DAC used to be applied utilizing CADENCE CMOS zero.18um technological know-how with give voltage 2.5 – 3.3V at a rate of 200MHz. The maximum vigor consumption of the 10bit FS-GDI DAC is 16.8mW. DNL is the deviation of the specific step dimension at each enters code from the excellent 1 LSB step[13-15].

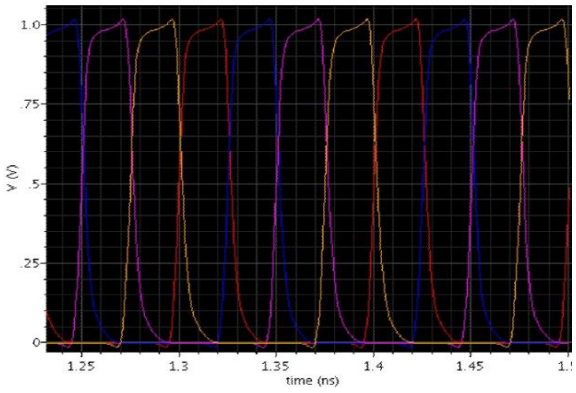

Fig. 9 Simulated Clock of 10-Bit FS-GDI DAC[13-15]

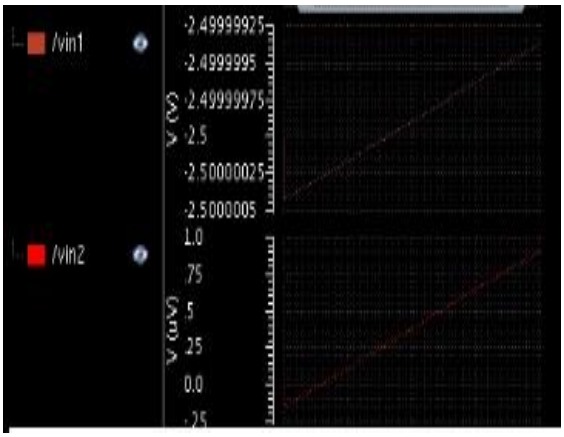

Fig. 10 Input Response Plot

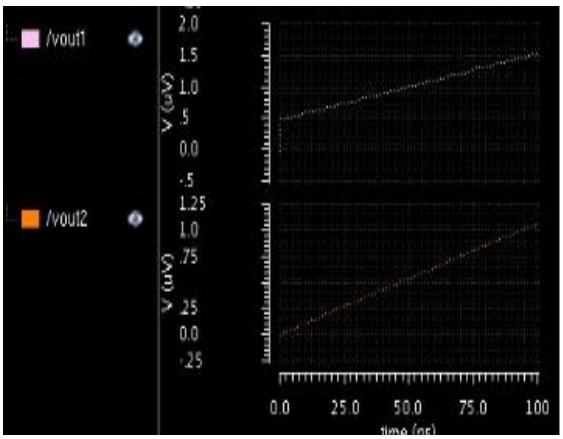

Fig. 11. Output Response Plot

DNL errors can result in summative noises and spurs afar quantization effects. INL is the variation of the actual voltage output from the ideal voltage output on a straight line drawn between the termination points of the transfer function. INL is calculated after offset and gain errors are removed. The DNL and INL of the proposed FS-GDI DAC were ±0.12 LSB and 0.01LSB, respectively. The Simulated Clock For Proposed FS-GDI DAC and the input and output response plot are figured in Fig.9., Fig.10. & Fig.11. respectively[13-15]. The comparison of results is shown in Fig. 12.

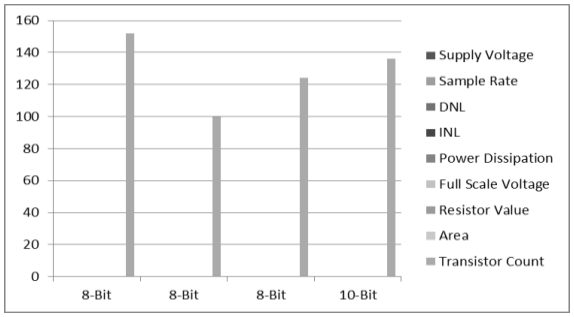

Fig.12. Comparison of Results

VI. CONCLUSION

In this paper, the 10-bit current-steering DAC was implemented using Full Swing GDI logic in CMOS process using CADENCE VIRTUOSO ENVIRONMENT to reduce the area and power dissipation. The proposed design of digital to analog converter successfully operates at a frequency range of 200MHz with varying voltage from 2.5 - 3.3V supply voltage level. A power consumption of 16.8mV, DNL and INL below 0.1LSB and 0.1LSB, which resembles low level compared with the existing system of DAC. The active area of the FS-GDI DAC is 0.004mm^2. The proposed 10-Bit FS-GDI DAC shows better results, when compared with existing designs regarding the parameters like DNL, INL and power consumption. The newly proposed scheme of 10-Bit FS-GDI DAC design is very much suitable for low power and high speed applications.

REFERENCES

[1] Yi S.C., An 8-bit current-steering digital to analog converter", International Journal of Electron Communication, (2012).

[2] Razavi B., Principle of data conversion system design. IEEE Press (1994).

[3] Van der Plas G.A.M., Vandenbussche J., Sansen W., Steyaert M.S.J, Gielen G.G.E., 14-bit intrinsic accuracy Q2 random walk CMOS DAC. IEEE Journal of Solid-State Circuits (2000).

[4] Deveugle J., Steyaert M.S.J., A 10-bit 250-MS/s binary- weighted current steering DAC, IEEE Journal of Solid-State Circuits (2006).

[5] Jurgen Deveugele, Steyaert. A 10-bit 250M-MS/s binary-weighted current steering DAC", IEEE Journal of Solid-State Circuits (2006).

[6] John Wilson and S. Sakthivel, Big Bang-Big Crunch Algorithm For Minimizing Power Consumption by Embedded Systems. International Journal of ECET (2014).

[7] Van den Bosch A., Borremans M.A.F., Steyaert M.S.J., Sansen W., A 10-bit 1G Sample/s Nyquist current-steering CMOS D/A converter. IEEE Journal of Solid-State Circuits (2001).

[8] Chen W., Bauwelinck J., Ossieur P., Qiu X.Z., Vandewege J., A current steering DAC architecture with novel switching scheme for GPON burstmode laser drivers. IEICE Transactions on Electronics (2007).

[9] Eisa S.M., Shehata K.A., Ragai H.F., Design and implementation of an 11-bit nonlinear interpolation DAC. In: DTIS International Conference on Design and test of integrated systems in nano-scale technology (2006).

[10] V. Suresh Babu and M.R. Biju, Novel Circuit Realizations of Neuron Activation Function and Its Derivative with Continuously Programmable Characteristics and Low Power Consumption. IJARET (2014).

[11] Chena C.Y., Current-mode digital-to-analog converter designed in hybrid architecture. International Journal of Electronics (2008).

[12] Lee D.H., Kuo T.H., Wen K.L., Low-cost 14-bit current-steering DAC with a randomized thermometer-coding method", IEEE Trans Circuits Systems (2009).

[13] Vishwanath Muddi and Sanjay Eligar. A High-Speed, Low Power Consumption D Flip-Flop For High Speed Phase Frequency Detector and Frequency Divider. International Journal of ECET (2014).

[14] A. Morgenshtein, A. Fish, I.A. Wagner, Gate-diffusion input (GDI)-a power efficient method for digital combinatorial circuits. IEEE Transactions on VLSI Systems (2002).

[15] A. Morgenshtein, I. Shwartz, A. Fish, Gate diffusion input (GDI) logic in standard CMOS nano-scale process, Proceedings of IEEE Convention of Electrical and Electronics Engineers in Israel (2010).