EFFICIENT IMPLEMENTATION OF DECODER USING MODIFIED SOFT DECODING ALGORITHM IN GOLAY (24,12) CODE

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ABSTRACT

Aim / Objective: The (24, 12) binary Golay code was a well-established rate-1/2 short block-length linear error detecting and correcting code with High performance.

Algorithm / Simulation: This paper investigates the design of an efficient low-complexity soft-decision decoding architecture for this Golay code. A new algorithm is introduced that takes a huge advantage of the code's properties to reduce and simplify the decoding process.

Findings & Results: The Simulation result shows that the proposed algorithm of Modified soft decision decoding achieves high performance rates with low processing cost. Here the decoder architecture is mentioned, and VLSI synthesis results are presented.

Applications: can be used in high speed cryptography systems

Keywords: ***Soft Decision, Golay Code, VLSI***

I. INTRODUCTION

The method of Forward Error Correction is a most critical non-hypothetical means for scholarly advantage to the BER functionalities, execution of capacity frameworks and computerized correspondence. The (23, 12, 7) parallel Golay code was a flawless double triple-mistake remedying code presented in 1949 by Golay1 with strong math properties. The summation of a general equality check bit creates the rate-1/2, self-double (24, 12) twofold Golay code which has discovered unfathomable applications either as a free code or as an internal code in combined coding systems[2, 3].

A tremendous numeral of choice logarithmic unraveling frameworks had examined throughout the decades (see case [3-5]). In dissimilitude to hard-choice decoders which utilize on parallel qualities, delicate choice decoders straightforwardly handle set of unquantized (or quantized on more than two levels practically speaking) specimen information at the yield of the coordinated channel, in this manner avoid the loss of data. Over the Additive White Gaussian Noise (AWGN) channel, delicate choice unraveling ceaselessly give up to 3 dB coding increase over hard-choice translating method, yet at the expense of expanded computational ensnarement.

Delicate choice interpreting engineering and calculations for the expanded Golay coding have likewise gotten a great deal of consideration [6,7] but the many-sided quality nature of stretched out Golay code makes us to consider the clubbing of delicate choice disentangling calculation with the essential Golay usefulness (24, 12), yet not very many decoder models had distributed. This paper is especially inscriptive, in requesting issue of planning a straightforward ≥ 5000 doors delicate choice decoder engineering with close most praising execution for the (24, 12) code.

The present delicate choice methodology depends on the interpreting calculation founded in[9,10]. This calculation is resolved to rate-1/2 straight codes having a generator lattice unflustered of an invertible subnetwork for the release part. A twofold re-encoding procedure is induced by Chase's algorithm[11] is utilized to make a rundown of competitor code (CC) words among which, the most comparable choice is held as the decoder choice[11,12,13,14]. A not very many number of blunder examples were appeared to be typically rich to accomplish near most ML[15,16] execution for short square codes. The overflow of the paper is complimented as takes after. Segment 2 explains about the diverse ways to deal with encode the (24, 12) Golay code. Area 3 explains the guideline and execution behind the proposed plan of delicate choice interpreting calculation. The outline of equipment productive decoder engineering with close ML execution is expounded in Section 4. Conclusions displayed in Section 5[1-15].

II. ENCODING USING GOLAY (24, 12) CODE

Since the presented, proposed reversed scheme of soft-decision decoder performs several re-encoding processes of the received data sequence, the first process is with the reviewing various encoding steps involved in the Golay code. The binary (24, 12) Golay code can be mentioned in a cyclic form as a residue code of quadratic function with generator polynomial **g(x) =x11+ x9+ x7+ x6+ x5+ x+1I**s explained in [4 & 16]. Thus an 11-stage shift-register followed by an accumulator can be used to perform systematic encoding of the (24, 12) Golay code in 12 clock periods.

The general property of the Golay code is given as follows[1-15].

1) The length of G24 is 24 and its dimension is 8.

2) A parity-check matrix for G24 is the 12 X 24 matrix H = [Aj I12].

3) The code G24 is self-dual, i.e., G24 = G24.

4) Another parity-check matrix for G24 is the 12 X 24 matrix H0 = [I12 jA] (= G

5) Another generator matrix for G24 is the 12 X 24 matrix G0 = [Aj I12] (= H).

6) The weight of every code word in G24 is a multiple of 4.

7) The code G24 has no code word of weight 4, so the minimum distance of G2 8.

8) The code G24 is an exactly three-error-correcting code.

An extra thought is that they quickly execute with rationale doors and the generator grid Gd with stretched out with the parallel learning vector d of the code. Since the Golay code is a self-double code, the generator lattice Gd in most effortless sort can be composed as Gd = [I_{12}, P] where I_{12} is the 12 x 12 personality

framework comparing to the 12 learning bits d, and where, P is a 12x12 invertible twofold grid that is utilized to produce the 12 equalities decide bits p. The individual code word c then peruses c = (d, p). From the self-twin property of the Golay code, P fulfills the property P-1 = P^t. Subsequently, inside the equivalent way that the 12-data co-ordinate d are utilized to register the equality bits p using the generator lattice Gs= [I_{12}, P], the 12 equality co-ordinates p will likewise be encoded utilizing the option generator network Gp = P-1 X Gd = [P^t, I_{12}] to get the data vector d. A third procedure makes utilization of the Cortex development. Cortex codes are a friends and family of self-double direct piece codes, which used to be initially displayed in[12]. As appeared in Fig. 1, they blend a dreadfully concise gatekeeper code E with a progression of altering the request to give the equality bits. On the off chance that the mummy code is self-double, the subsequent Cortex code acquires from the self-twin property[13].

The Cortex constitution likened to the Golay code is demonstrated in Fig. 2. It is outlined arranged on the (8, 4, 4) quickened Hamming code which is meant H. The 12 ability bits d are isolated into three pieces of every last 4 bits. Every last piece is encoded with the guide of the (8, 4, 4) code to give four equality bits, and the efficient bits are further disposed of. The grouping of 12 equality bits is then shambled by utilizing a good exchange highlights, and the whole framework is rehashed for basically 3 events to create the equality bits p as required.

The codeword is at long last procured by method for linking the 12 efficient bits d with the 12 last equality bits p. Curiously, the (8,4,4) quickened Hamming code utilized as a developing piece for planning the proposed Golay code in Cortex structure, which can likewise be one of a kind as a Cortex code. The comparing Cortex structure is demonstrated in Fig. 3. It is planned headquartered on the (4, 2, 2) Hadamard code as demonstrated in decide above and furthermore introduced in [14-16]. This paper presents about the Cortex engineering for encoding the natural (24, 12) Golay code[1-15].

III. MODIFIED SOFT DECISION DECODING OF THE (24, 12) GOLAY CODE

The traditional system is reversed in the proposed scheme; hence a ML soft-decision decoding is known to offer the best decoding performance but is usually computationally intractable for most codes of practical interest[14,15]. Brute-force ML decoding of the Golay code requires correlating the received word with each of the 2^{12}=4096 candidate code words, which is computationally feasible yet intensive. A smarter approach would be to apply a variant of the Viterbi algorithm to the tail biting trellis representation of the Golay code introduced in[1-15]. However, despite of its simplicity, this approach is not the most sought after one when low gate count and very high data rate are sought [1-15].

For these reasons, we have chosen to focus rather on the simple and efficient algorithm initiated in[10] this algorithm can be used to any order of self-dual codes, and is notably attractive for short codes, which it offers mere near-ML staging at low decoding complexity. The algorithm operates as follows. A list of V_{Ts} candidate code words is obtained by applying binary test patterns to the *k* message bits obtained by taking a hard-decision at the collected data / information series, and then re-encoding the resulting candidate sequence.

As suggested by Chase in[11], the test patterns V_{Ts} attempt to correct the most likely errors patterns confined in the least reliable positions in the collected data / information series. The same procedure can be used in parallel to the *k* parity bits, by reversing the encoding eqns. to re-calculate the *k* message bits from the *k* parity bits. This results in a second list of V_{Tp} candidate code words. The decoder finally selects the candidate code word at minimum distance i.e., Euclidean distance at the maximum correlation metric from the collected word. Bit Error Rate (BER) performance versus Signal to Noise Ratio (SNR) of this algorithm for the (24, 12) Golay code using 8-bit quantization is presented for different numbers of test patterns of $V_T = V_{Ts} + V_{Tp}$. BPSK transmission over AWGN is assumed. We observe that 32 i.e., (16+16) test patterns are adequate to obtain a close call to ML performance within the range from 0.1to0.2 dB in the executed BER range. The distinguished architecture is introduced in the next section uses a total of 24 (12+12) test patterns, thereby effectively attaining ML performance.

IV. RESULTS AND DISSCUSSION OF SOFT DECISION DECODING OF GOLAY (24, 12)

Despite of its short block length, developing a new scheme of low complexity Soft decision decoding structure for the Golay code that is biddable to very high data rates stands like a hurdle. Here, we narrated a digital implementation fitted to the soft-decision decoding algorithm, which are investigated in the previous Sections. The decoder operates on soft decisive inputs quantized at q=3 bits (+ sign bit). A sum of $V_T = V_{Ts} + V_{Tp}$ = 12+12 = 24 candidate code words is used to generate the total decoder decision. The 2x12 error patterns are chosen to correct the most probable errors located in the architecture, which is $L_{rs} = L_{rp}$ = 5 least authentic positions in both the Data parts and parity parts of the collected vector.

The analogous architecture is inspired by[14] and is shown in Fig. 6. It contains four major blocks known as reception block, processing block, transmission block and control block. The inner of the reception block, the n=24 soft symbols of the collected word are processed in a sequential manner. This block first spots successively the L_{rs} and L_{rp} least reliable positions within the ordered and parity parts of the collected word, respectively. In parallel, a SIPO shift-register study and memorizes sequentially the 12 soft samples of the collected word. The processing block comprises three major functions; they are, first is error patterns generation from the sign bits of the collected word by testing different possibilities of 0s and 1s in the least dependable bit positions. Then, these generated error patterns are summed (modulo-2) to the Data / parity sequence and the following sequence is re-encoded to fabricate a code word which achieved a correlation metric.

Finally, a choice function comparator spots the most desirable code word within the 24 candidate code words input list. Note that this process is understood clearly in parallel for the data and the parity parts of the collected word. Moreover, the metric of every candidate code word is enumerated from the 12 soft symbols provided using the shift register SIPO; at last, the transmission t_x block is self-possessed merely of a PISO shift register, used to deliver continuously the methodical bits of the decoder decision in the output. The three precursory blocks are superintended by a control block. In this proposed design, this task is realized by a 5-bit counter that conjures the essential control signals. As shown in Fig. 6, the soft decoder architecture scheme is designed in two pipelining channel stages: reception transmission and processing transmission. The first stage often flows in a series of 12 collected soft symbols in duration of 24 clock periods. In the second stage, the 12+12 candidate code words are generated, scored and compared. Finally, the 12 decoded data bits are delivered sequentially in 12 clock periods. The latency *L* of a decoder usually depends on the total number of channeled pipeline stages and on the code word length *n*. For the proposed decoder architecture, the resulting latency is $L=2n=24$ clock symbols. Logic synthesis has been performed using the CADENCE 0.18µm CMOS process ASIC target was considered. Thus, the reversed scheme is high efficient with a frequency of 400 MHz.

The results are presented in Table 1, which presents the complexity of each function in a soft decoder. We observe that the proposed soft decision decoding architecture requires about 4000 equivalent gates. In this proposed reverse scheme, the maximum data rate is ≥ 450 Mb/s. Thus, the proposed soft decoder is less complex than the parallel hard-decision decoder at the core of the soft-decision decoder architecture described in[6] and we achieved a date rate of 500 Mb/s.

V. CONCLUSION

Soft-decision decoding of Golay codes has been investigated and decoder architecture has been presented. The proposed design depends on a devoted decoding algorithm which exploits the code belongings to reach near-ML performance by a minimal number of error patterns. The simulation result shows the benefits of the proposed high efficient decoding algorithm.

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$$\begin{bmatrix}
1&0&0&0&0&0&0&0&0&0&0&0&1&1&0&1&1&1&0&0&0&1&0&1\\
0&1&0&0&0&0&0&0&0&0&0&0&0&1&1&0&1&1&1&0&0&0&1&1\\
0&0&1&0&0&0&0&0&0&0&0&0&1&0&1&1&0&1&1&1&0&0&0&1\\
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0&0&0&0&0&0&0&0&0&0&0&1&1&1&1&1&1&1&1&1&1&1&1&0
\end{bmatrix}$$

Figure 1 Proposed Parity Check Matrix for Golay (24, 12) Code[1-15]

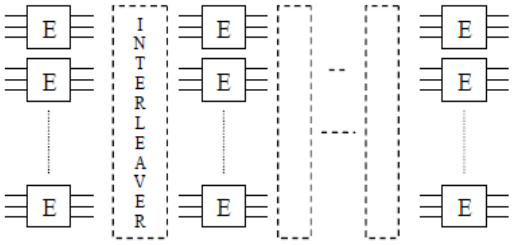

Figure 2 General Cortex encoding scheme build from Elementary code E[1-15]

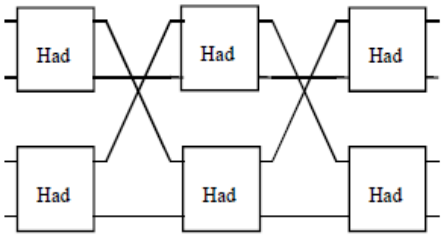

Figure 3 Cortex encoding architecture for the (8, 4, 4) extended Hamming code[1-15]

Code	Weight-4 codewords (in decimal)													
C_1	29	39	58	78	83	105	116	139	150	172	177	197	216	226
$C'_{(8)}$	23	43	60	77	90	102	113	142	153	165	178	195	212	232
$C'_{(2)}$	27	46	53	77	86	99	120	135	156	169	178	202	209	228
$C'_{(3)}$	30	45	51	75	85	102	120	135	153	170	180	204	210	225
$C'_{(4)}$	23	46	57	75	92	101	114	141	154	163	180	198	209	232
$C'_{(5)}$	30	43	53	71	89	108	114	141	147	166	184	202	212	225
$C'_{(6)}$	27	45	54	71	92	106	113	142	149	163	184	201	210	228
$C'_{(7)}$	15	51	60	86	89	101	106	149	154	166	169	195	204	240
$C'_{(8)}$	15	54	57	85	90	99	108	147	156	165	170	198	201	240

Figure 4 Generated Code words for Golay (24, 12) Code[1-15]

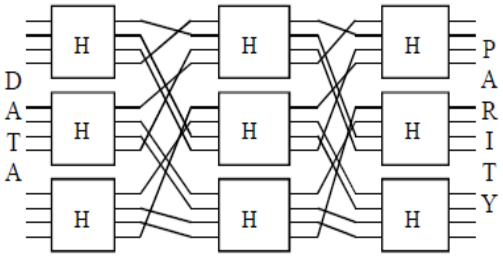

Figure 5 The Cortex Architecture for Golay (24, 12) Code[1-15]

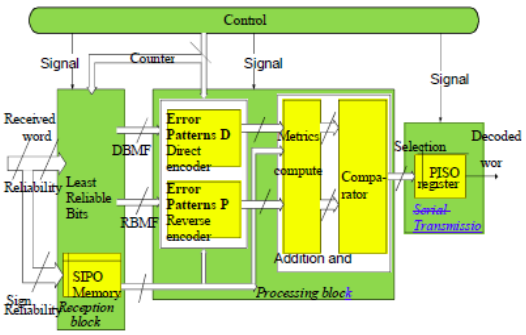

Figure 6 Proposed Modified Scheme of Soft Decision Architecture for Golay (24, 12)[1-15]

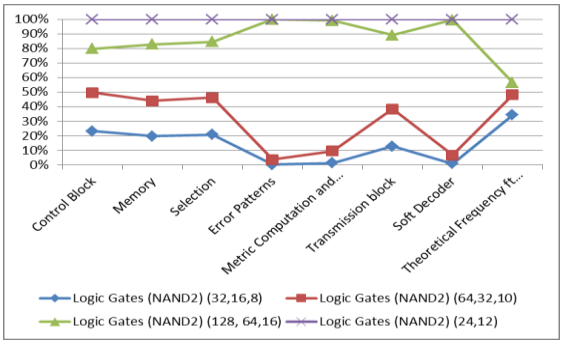

Figure 7 Comparison of Simulation Results

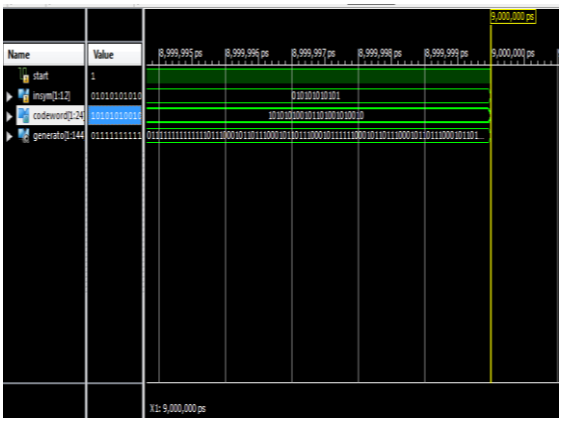

Figure 8 Encoding using Golay (24, 12)

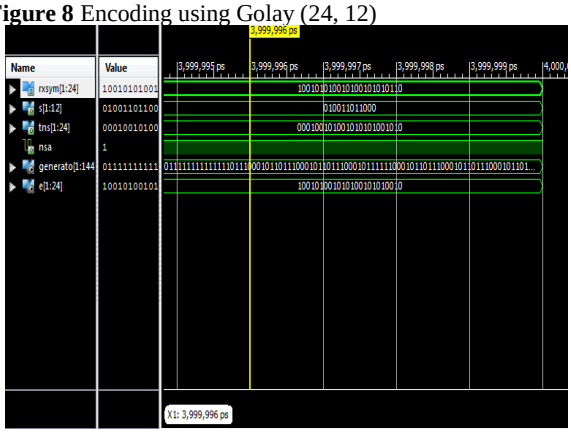

Figure 9 Efficient Decoding using Soft-Decision for Golay (24, 12)

Table 1 Simulation results of the Proposed Scheme

Parameters	Logic Gates (NAND)			
Cortex Code	(128,64,16)	(64,32,10)	(32,16,8)	(24,12)
Control Block	107	94	82	72
Memory	3260	2036	1634	1432
Selection	1815	1201	974	732
Error Patterns	668364	24570	248	137
Metric Computation & Selection	509680	47809	6327	5221
Transmission Block	404	202	101	86
Soft Decoder	1183246	75912	9366	7366
Frequency (MHz)	77	128	315	400