DESIGN AND TESTABILITY OF Z-TERNARY CONTENT ADDRESSABLE MEMORY LOGIC

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ABSTRACT

The emerging technology using Field Programmable Gate Arrays (FPGA's) is the leading architectures with look-up tables (LUT's) based design plays the major role in the chip design. The memory unit and controller are the basic units and it performs the operation based on the lookup table methods. The logic circuit is designed based on requirements. The Ternary content addressable memories (TCAMs) are hardware-based parallel lookup table design with masking capability in bit level. So it is attractive for applications such as network routing and packet forwarding. The high power consumption is one of the major limitations faced by TCAM designers. This proposed design is based on the circuit techniques aiming to reduce Ternary Content Addressable Memory power consume. The Traditional TCAM table and its hybrid partitions are implemented based on the testing and verification of memory unit. The method is implemented using the normal architecture analysis. The ternary logics are implemented in shift registers, Input output

Keywords: TCAM, LUT,Bit level Logic & DFT

1. INTRODUCTION

Ever since the invention of the transistor, the semiconductor industry has grown into diverse applications areas. These range from entertainment electronics on one side to space applications on the other. Regardless of the application areas, the quality and reliability demands for semiconductor devices have significantly increased. Increasing system complexity also requires higher quality manufacturing from IC suppliers. On the weak hand, market economics have forced pure digital integrated circuits to incorporate embedded memories, as well as analog blocks. Hence, an IC package might include all the functional blocks of a microcontroller or microprocessor, including memories and analog interfaces. This results in a drama-tic change in the case of memories.

High packaging density, standard manufacturing process implementation and the dynamic nature of process operations make memories susceptible to a variety of manufacturing process defects. Testing is necessary to assure device reliability and quality. The Memories store the values in ones and zeros format. These ones and zeros can be stored or retrieved. Most memories store the data inputs to some location. Accessing the memory location from other memory locations is simple by selecting a set of x-y coordinates. Content Addressable Memory (CAM) is a type of memory element that is present in many chips along with other memories.

The main difference between a Content Addressable Memory and a Random Access Memory (RAM) is that, in a RAM the user supplies the address and gets back the data and in a CAM the user supplies the data and gets back the address. Due to the architectural difference between CAM and RAM, testing of these memories differ. When compared to RAM, a CAM has three modes of operation, namely: compare, read and write. Due to this, fault models and test patterns chosen for a CAM is different when compared with RAM.

2. DEFINITION OF TESTING

Testing is necessary to determine if a product has been manufactured correctly not. Testing is possible when a known input stimulus is applied to a device in a known state, and when response can be evaluated, as shown in Figure 1. When a new IC chip is designed and fabricated for the first time, testing is used to verify the correctness of the design and the test procedure. This is called verification or characterization testing. In this case, the new chip is verified for correct design and operational specifications. Successful verification testing usually results in some good chips. Large-scale manufacturing generally requires manufacturing testing. At the customer end, the manufactured chips may be tested again to ensure quality.

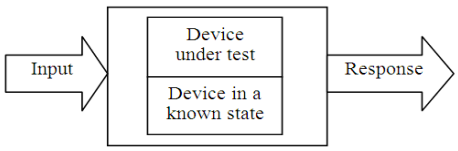

Figure 1: Definition of Testing

The actual test selection process is based on the manufacturing level being tested. In manufacturing, each chip is subjected to two types of tests - Parametric test and Functional Tests. DC Parametric tests include open test, short test, leakage test, and maximum current test. The propagation test includes the propagation delay, setup time, hold time, its speed, and access time test [1]. These tests are usually technology dependent; it depends upon the predefined tasks. The physical verification and functional tests consist of input vectors and the corresponding responses as a result. Proper operation of a verified design can be checked by testing the internal chip nodes. Memory tests are functional. These tests are designed to check functional attributes such as address decoder operation, cell coupling, column and row decoder coupling, write recovery and refresh. Functional tests should cover a very high percentage of modeled faults in logic circuits.

Memory tests can be divided into concurrent and non-concurrent tests. Concurrent tests detect faults dur-

ing normal system operation [2], whereas non-concurrent tests require suspension of normal system operation to test the faults. For testing memories at the wafer and chip level, non-concurrent tests are preferred because they can be designed for any desired fault model. The increased emphasis on reducing the defect level of shipped memory parts, therefore, necessitates the need for very high quality in non-concurrent tests. Usually, not a single test, but a series of tests are required due to the diversity in fault models. The proper selection of the tests to be performed, hence strongly depends on the fault models of the memory.

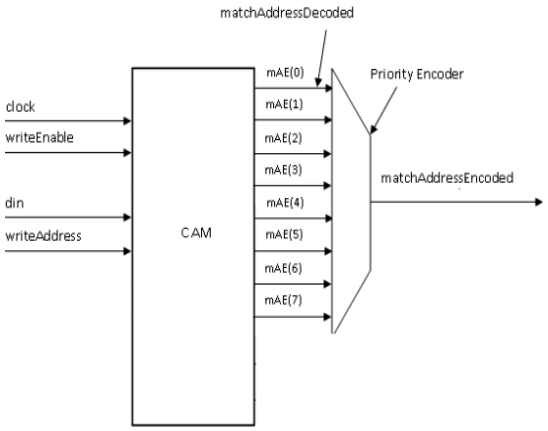

Figure 2: Simple CAM

Memory is a major component of a digital computer and is present in a large proportion of all digital systems. Figure 2 shows the simple architecture of CAM. Memory is a collection of binary storage cells capable of storing binary information. In addition to these cells, memory contains electronic circuits for storing and retrieving information. The information can be retrieved from the memory in the form of ones and zeros. Semiconductor memory is usually considered the most vital microelectronic component of digital logic system design. Semiconductor memories are characterized as volatile and nonvolatile memory devices.

3. Content Addressable Memory

A CAM allows a fast-concurrent search of input data into the memory. This is the main advantage of a CAM over a RAM. The CAM write mode is comparable to a RAM, but the CAM read mode is different [3]. In a RAM, the word in a specific location is read by the address. In a CAM, the data on the input is looking for a match. When a match is found, the output is the address in the array. The number of address lines limits a RAMs data size. CAM's can be used in applications where search time is very critical and must be very short. Content Addressable Memories (CAMs) play a key role in many modem digital systems.

CAMs are widely used wherever fast parallel search operations are required. Some examples of CAMs found on modem processors are translation-look a side buffers (TLBs), branch prediction buffers, branch target buffers and cache tags.

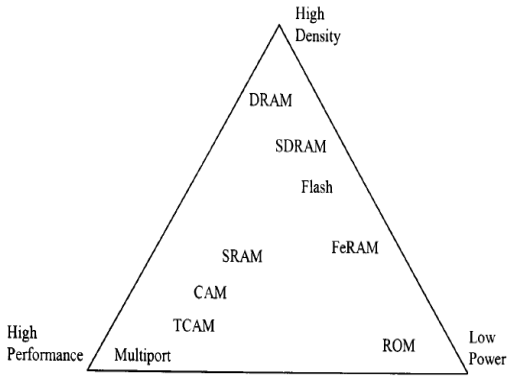

Figure 3: Continuous of power and Performance

Memory tests should deliver the best fault coverage possible given a certain test time. The tests are based on fault models and try to have complete coverage for particular fault models. The purpose of a fault model is to simplify the testing procedure and reduce its cost, while still retaining the capability of detecting the presence of the modeled fault.

3.1 Memory fault models

Physical examination of memory is not possible. The only other possible testing mechanism is to compare logical behavior of faulty memory against good memory. This requires modeling of the physical faults as logical faults. Modeling faults as logical faults makes this approach independent of the technology and manufacturing process. One limitation is that it may not be possible to relate a failure detected by a test to the actual physical defect, due to the high level of fault modeling. Memory faults can be modeled using one of the following memory fault models. In a behavioral model, all possible combinations of memory contents are considered. A functional model is more commonly used compared to behavioral, logical, electrical and geometric models. The advantage of using functional models is that they have enough detail of data paths and adjacent wiring runs in the memory to model the faults to be tested.

Memory fault models are faults modeled in the memory block that are single cell stuck-at [0, l] faults, pattern sensitive faults, cell coupling faults and single stuck-at faults in the address decoder logic. Functional fault modeling for CAM cells is based on physical defects, such as shorts between two nodes and transistors stuck-on and stuck open faults. Functional faults can be cell stuck, data line stuck, open in data line, short between data line, open in address line, short between address lines.

In stuck-at faults, the logic value of a cell or line is always ' 1 ' (SA1) or '0' (SA0). If a cell or a line fails to undergo a 0-1 or 1-0 transition then it is called a transition fault (TF). A coupling fault (CF) between two cells occurs when the logic value of a cell is influenced by the content of, or operation on, another cell. A neighborhood pattern sensitive fault (NPSF) occurs when the content of a cell is influenced by the content of other cells in the memory. Any fault that affects the address decoder operation is an address decoder fault.

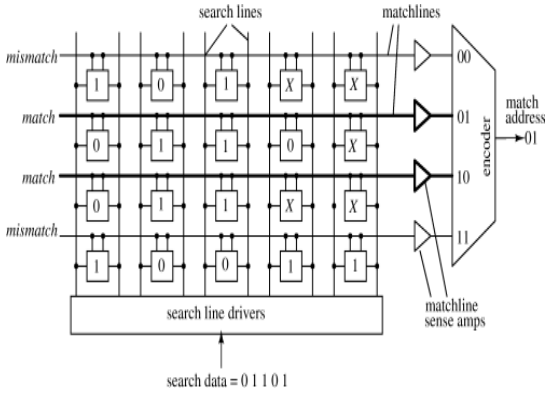

Figure 4: Block diagram of a CAM

There are three basic operations for the CAM: Read, write and compare (Match). These operations depend on the values of word line (WL) and bit line pair. The block diagram of a CAM is depicted in Fig. 4. The read and write operations are similar to that of a RAM. The word line (WL) is asserted only when a read signal or write operation to the RAM is considered. The read operation returns the data associated with the matched word. In a read operation, the state of the memory cell must be determined through the access transistors T1 and T2 without upsetting the data in the cell.

Table I Comparison between CAM and TCAM

SI. No	CAM	TCAM
1	CAM tables pro-vide only two res-ults: 0 (true) or 1 (false).	Ternary CAMs support storing of zero, one, or don't care bit (0, 1, X).
2	CAM is most useful for building tables that search on exact matches such as MAC address tables.	Ternary CAMs are presently the dominant CAM since longest-prefix routing is the Internet standard

4. DESIGN, SIMULATION AND TESTING OF CAM

Xilinx integrated software environment is a design tool for digital circuit design, FPGA design and other programmable design technologies. It is an interactive tool for design entry, synthesis and verification capabilities. The design can be started with a number of source types like HDL (Verilog or VHDL), Schematic Design, EDIF, State machines. The functionality of these sources is verified using the integrated simulation capabilities including Modelsim and HDL test bench generator. The Xilinx implementation tool continues the process into a placed and routed FPGA and finally produces a bit stream for device configuration.

The content addressable memory is designed using Verilog HDL. The content addressable memory module consists of a hierarchy of blocks performing different functions. The hierarchy includes a top-level block consisting of sub-blocks. The first step in the functional verification of the device is creating a top level hardware description model. The level of abstraction for modeling a circuit depends on the purpose for which the model is intended. A behavioral model is the most appropriate model for verification and functional simulation of complex hardware units. But creating a single behavioral model for such a large design, which includes a lot of blocks and features, is not feasible. This problem is countered by describing individual smaller modules in Verilog HDL. Using Verilog HDL, behaviorral models of different modules can be written and these models can be extracted in a top level net list extraction. Figure 5 shows the proposed block representation.

The ternary logics are defined as follows.

- B1,B2=00-Shift Register
- B1,B2=01-PRPG (pattern generator)
- B1,B2=10-Normal System Mode
- B1,B2=11-Multiple-input signature registers

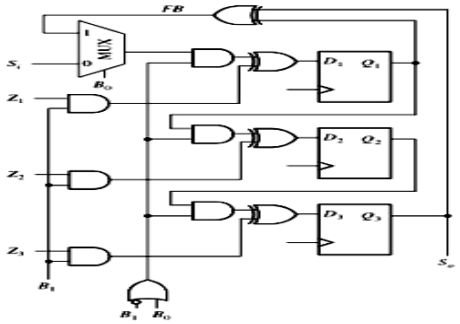

Figure 5: Proposed block Representation

Design for Test is a technique, which indicates a design to become the testable after production. It is the extra logic which is designed in the normal design, during the design process, which helps its post-production testing. The Post-production testing is important because, the process of manufacturing is not 100% error free. The block representation Figure 5 shows the proposed design is made for testing. Hence it is necessary to test the fault in the designed model. If there is any defect in silicon which results in errors and it produces the fault in the physical devices. Hence it is important to provide the fault modeling and analyze the result with lookup table based design.

The complexity of designed memory cell and array architecture is rapidly intending with the introduction of advanced technologies. The high level of system functional integration on silicon is requiring higher density and more complex memories. Testing of these hardly accessible externally a memory is further complicated due to different test requirements of SRAM, DRAM, Flash, ROM and CAM. Each of these has different density and power requirements. Figure 3 shows relative locations of several memory types based on performance, power and density.

Ternary content addressable memories (TCAMs) are gaining importance in high-speed lookup-intensive applications. However, the high cost and power consumption are limiting their popularity and versatility. TCAM testing is also time consuming due to the complex integration of logic and memory [6]. TCAMs have certain drawbacks such as low storage density, low

scalability, relatively slow access time complex circuitry, and are very expensive.

Ternary content addressable memory (TCAM) allows its access to memory by searched the contents rather than the address and a memory location among matches is sent to the output in a constant time. A typical TCAM cell has two static random access memory (SRAM) cells and a comparison circuitry and has the ability to store three states − 0, 1, and U where x is don't care or it may be undefined state.

The x state is always regarded as matched irrespective of the input bit. The constant time search of TCAM makes it a suitable candidate in different applications such as network routers, data compression, real-time pattern matching in virus-detection, and image processing [4].

5. RESULTS & DISCUSSION

The stored keys contain don't care bits in the bit positions used for hashing, then such keys must be duplicated in multiple buckets, which need increased capacity [5]. On the other hand, if the search key contains don't care bits which are taken by the hash function, multiple buckets must be accessed that results in performance degradation. The Table 2 shows the logical table for Ternary and binary representation with respect to state.

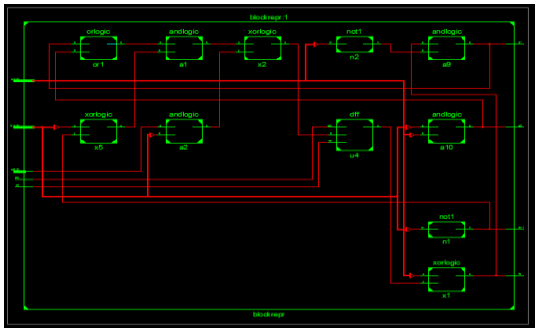

Figure 6: Register Transfer Logic for block Representation

Table II logical Table for Ternary

SI. No	Ternary logic	Binary	State
1	00	000	0
2	01	010	1
3	10	100	X
4	11	ZZZ	undefined

Several algorithms and techniques have been proposed recently to accelerate regular expression matching and enable deep packet inspection at line rate. This work aims to provide a comprehensive practical evaluation of existing techniques, extending them and analyzing their compatibility. The study focuses on two hardware architectures: memory-based ASICs and FPGAs [7].

In digital circuit design, the register-transfer level (RTL) is a design abstraction which decides a synchronous digital circuit in terms of the flow of digital signals (data) between logical operations and the hardware registers performed on these signals. The basic transfer function of designed CAM is depicted in Figure 6. The gate delay shows the 6.901ns with net delay 5.463ns. To take multiple cycles for a lookup, thus making CAM latency even longer. With the inclusion of priority encoder, latency becomes four clock cycles. Latency can be easily compromised if through-put is achieved. The throughput of the proposed TCAM is one-word comparison per clock cycle.

Figure 7 shows the ZTCAM logical functions which are done previously with the help of internal architecture design. It describes the logics such as 00, 01, 10 and an undefined state 11. The ZZ also assigned as an undefined state.

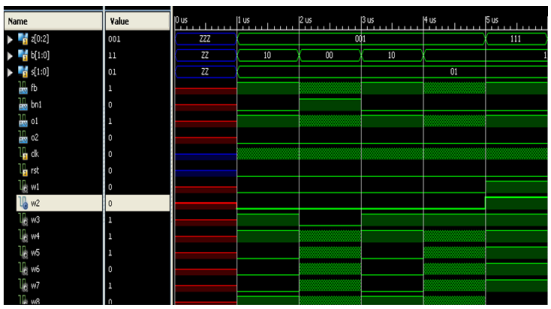

Figure 7: Logical units with four logic states

The logical units consist of internal controller, content addressable memory and a memory array it is shown in Figure 8 as RTL view.

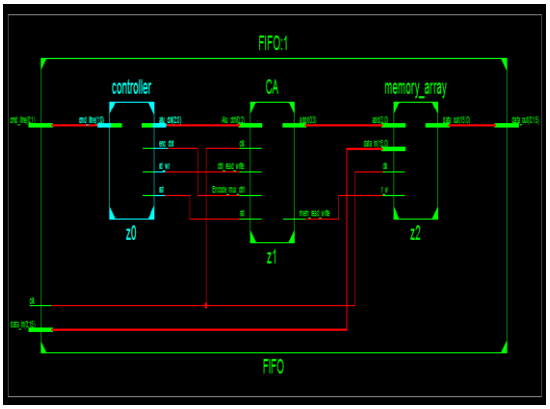

Figure 8: RTL view for content addressable memory

The Figure 9 shows the value of 000 for 00, 010 for 01,100 for 10 and ZZZ for undefined state 11. The result discusses the actual detail description of each content is taken or retrieval from the 3 bit address. The classical TCAM table along columns and rows into hybrid TCAM sub tables while represented is done and a new block representation is created [4].

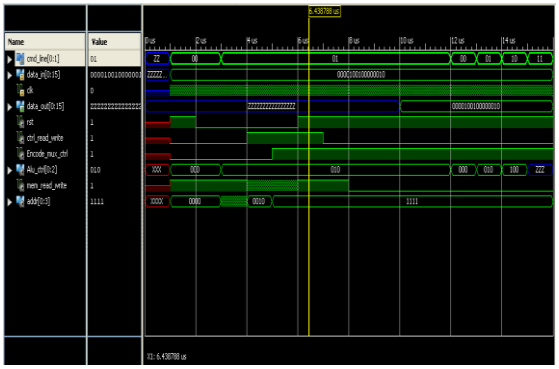

Figure 9: Output for content Addressable Memory

6. CONCLUSION

TCAMs are gaining importance in high speed look-up-intensive applications. However, the high-power consumption of TCAMs is limiting their popularity and versatility. A reusable verification Content addressable memory has been designed, analyzed and tested for different logical operations in this paper. The content addressable memory is divided into two parts: storage and comparison parts. Only the faults affecting the comparison part has been considered. The faults affecting the comparison part is modeled using fault models and tested using a novel test set power consumption using Xilinx Xpower Analyzer. The simulation result shows the logical operations for several stages with minimum internal events.

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