

## FULL CUSTOM LAYOUT OPTIMIZATION TECHNIQUES

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### ABSTRACT

Design of an integrated circuit layout is said to be the characterization of the components and elements of the integrated circuit in 3-dimension in geometrical models which represents the silicon layers, oxide layers, metal and polysilicon. Optimizing the layout helps in producing less parasitic effects, interconnect delays, power dissipation and signal integrity in an IC. The proposed work reduces total layout area of the application by incorporating following methods together: 1) depletion sharing, 2) minimum distance rule and 3) different metal layers. The proposed technique is practiced on 40 transistor D-flip flop[1] layout using Cadence® virtuoso® 64 tool. On using the minimum distance rule method along with depletion sharing the total layout area is reduced by 71.60% and on combining all the three methods area reduces by 73.44% with reference to schematic driven layout of example circuitry. In proposed layout, in order to subdue the reliability issue, single vias are replaced with double vias wherever possible. Simulation after post layout is done and the corresponding power calculation has been identified for the layout of the example circuitry and results clearly say that total layout area reduction is reducing the power consumption directly in total.

*Index Terms*— Layout area, Area optimization, Depletion sharing, D-flipflop, Layout optimization, Metal layers.

### I. INTRODUCTION

The trend of reduced area and power has got its interest among the VLSI designers and different techniques are coming up for the same. In general, many VLSI applications are designed to have high processing speed and reduced power consumption. To produce an economical and cost-effective design for an application, area utilization has to be efficient. This leads us to improve the integration density. In full custom ASIC design, the first step is to describe the specification. In accordance with the specifications and functionality quoted, the chip is designed.

The schematic is created with Cadence® virtuoso® tool with the required specifications. The required analyzes are performed after designing the circuit to check its functionality. The schematic is then transformed into geometrical representation, called layout using Cadence® layout editor. The interconnections are done after the components placement and checked for errors. During fabrication, the data from the layout is reformed into photolithographic masks and finally the chip is designed, packed and tested.

Layout optimization is considered as one crucial factor in concluding the IC performance. The design complexity and handling capability demand introduces more challenges in improving the layout.

Allocation of white space in congested regions is one method to work on without compromising much and simultaneously improving the aspect ratio. Wirelength and critical area can be reduced effectively with robust and powerful routers. Wirelength can be reduced effectively on placing the components effectively [2].

Using bending connections, i.e., introducing jogs [1] in layout wherever possible reduced the white space in the layout. The rout ability optimization methods described may not give optimal results in some cases [3]. The routing algorithm proposed to bring changes in routing area than the logic area, due to the alteration flexibility in the routing area [6]. But, this approach toward routing area gives lesser yield.

The technique for repartitioning proposed to provide significant improvement in the rout-ability without inc-

reasing the congestion [4]. Robustness of the layout increases, using additional vias, shifting the wire connections and increasing the wire thickness [5,7].

This research work presents the methods by which the total area of the layout is reduced by decreasing the white space present in the layout. A 40 transistor D-flip flop is chosen as an example circuitry to implement and check the same. Reliability in layout also has been taken care.

### II. METHODOLOGY

Schematic of the example circuit is created using Cadence® virtuoso® 64 and connections are checked for errors. The schematic is analyzed to check whether all specifications match. Layout is created for the circuit using Cadence® layout editor. The interconnections are made using low metal layer for signal routing and high metal layers for power routing lines in order to reduce IR drop.

On completion of the layout, following physical checks are performed. 1) DRC (Design Rule Checking), to check the design rule such as metal layers distance, contacts, etc. 2) LVS (Layout Versus Schematic), to check whether the layout matches with the schematic. It checks for open and short errors.

The proposed methodologies are applied in succession to reduce the area. To increase the layout reliability, single vias are replaced with double vias without any new violations, wherever possible. Post layout simulation has been performed to check the power.

### III. PROPOSED WORK

A D-flip flop with 40-transistor is taken as an example circuitry. Schematic for example circuitry is designed using Cadence® virtuoso® schematic editor and proceeded with layout using layout xl editor. Fig.1. shows schematic of the D-flip flop.

In this research work, three methods called 1) depletion sharing, 2) minimum distance rule and 3) different metal layers are implemented to reduce the white space which are present in the layout area.

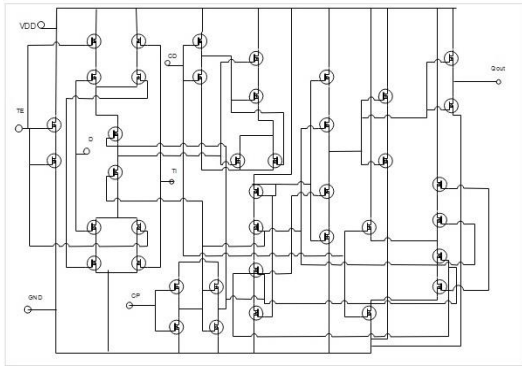


Fig. 1. Schematic of the D-flip flop

**A. Depletion Sharing**

Depletion sharing is a method, in which when two transistors with same terminal connections exist, they are merged together instead of using metal layers to connect the two transistors. Thus, this eliminates the unwanted space engrossed by wires.

**B. Minimum distance rule**

Minimum distance rule determines the minimum distance that must be maintained between the two objects in the layout. Minimum distance rule describes few constraints that are to be maintained by the designers for an efficient area optimization [6].

Fig. 3 shows the layout using depletion sharing and minimum distance rule.

Here are some of the minimum distance rules followed in cadence virtuoso in 180nm technology:

- Spacing between poly to poly:  $\geq 0.3 \mu\text{m}$ .

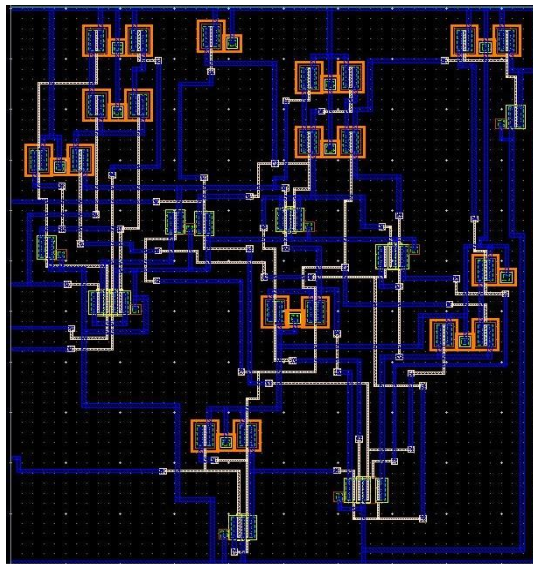


Fig.2. Schematic Driven Layout(SDL) of the D-flip flop(reference).

- Spacing between metal to metal:  $\geq 0.3 \mu\text{m}$ .
- Spacing between N-well to oxide:  $\geq 0.5 \mu\text{m}$ .
- Spacing between N-well to N-well:  $\geq 1 \mu\text{m}$ .
- Spacing between Nimp to Nimp:  $\geq 0.4 \mu\text{m}$ .

If the stated distance is not maintained between the objects in the layout, it would result in DRC error. To achieve a better layout design, it is good to arrange the objects according to the distance specified or slightly more. On applying this technique, area of the layout was reduced.

**C. Different Metal Layers**

On using different metal layers, area can be reduced further as a metal layers can be overlaid over other without overlapping with the same metal layer, if designed effectively. In the proposed work three different metal layers are used. The high metal layers (metal 3) being used for power supply and the metal 2 for horizontal connections and metal 1 for vertical connections. Fig. 4 shows the layout designed using different metal layers.

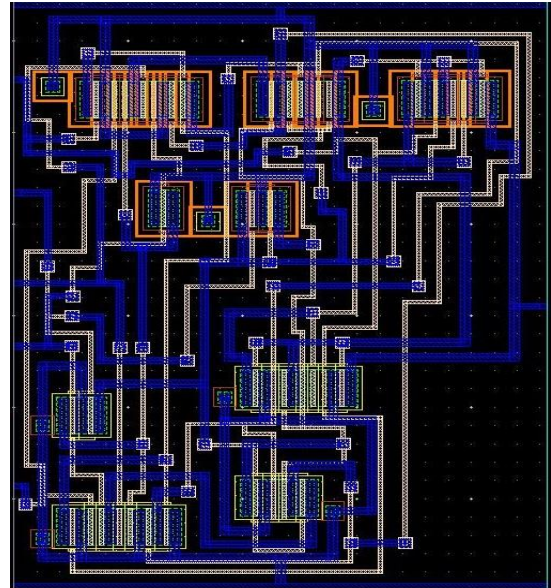


Fig.3. Layout of D-flip flop using depletion sharing and minimum distance rule.

**IV.RESULTS AND DISCUSSIONS**

The main focus of this paper is to reduce the unwanted white space present in the layout which significantly reduces the area. A 40-transistor D-flip flop is taken as a sample circuitry to analyse the same. The example circuit, D-flip flop carries few circuits which includes a NOR circuit, CMOS latch [3]. The layout for the reference circuit occupies an area of  $2634.82175 \mu\text{m}^2$ . On applying the minimum distance rule along with depletion sharing technique to the schematic driven layout, area is reduced to  $748.251 \mu\text{m}^2$ .

Finally, on using different layers in the schematic driven layout, the area is further reduced. Three different metal layers are used. The high metal layer (i.e.) Metal 3 is used for power supply and metal 2 is used for horizontal connections in the layout and metal 1 is used for vertical connections.

This technique further reduces the area. The total area reduced on applying all three techniques is  $699.5973 \mu\text{m}^2$ , which is 73.44% less than the reference layout. The area occupied after each method implemation and the reduction in percentage is shown in TABLE I.

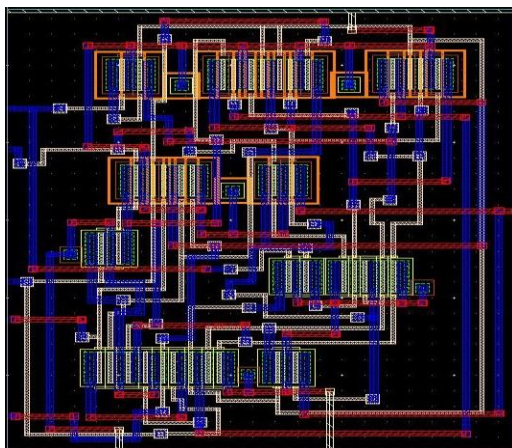


Fig.4. Layout using different metal layers.

Table 1 shows area occupied in each layout design and percentage reduction of the area

TABLE II. POWER CALCULATION OF DIFFERENT LAYOUT AFTER POST SIMULATION

Method	Power after post simulation
Reference layout	41.55 $\mu$ W
Layout using depletion sharing and minimum distance rule	37.46 $\mu$ W
Layout after using depletion sharing, minimum distance rule and different metal layers.	35.51 $\mu$ W

On implementing the proposed methods, reliability issue may occur. To resolve the reliability issue occurred, single vias in the layout are replaced with double vias, wherever possible. Layouts designed with double vias connections using depletion sharing and minimum distance rule is shown in Fig. 5 and different metal layers is shown in and Fig. 6.

Post simulation and power calculation after post simulation has been performed. The power analyses results show that on reducing the area, the consumption of the power is also reduced. The post simulation power calculation has been tabulated in the TABLE II.

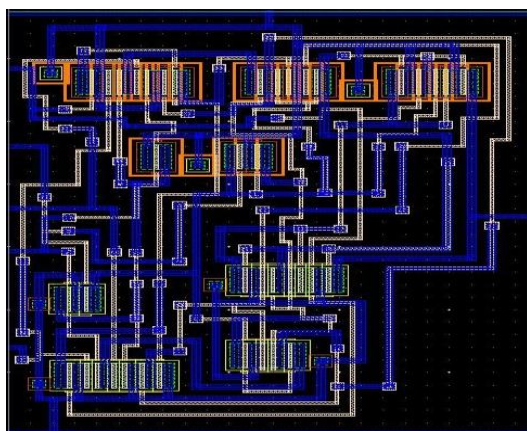


Fig.5: Layout with double via connection (using depletion sharing and minimum distance rule).

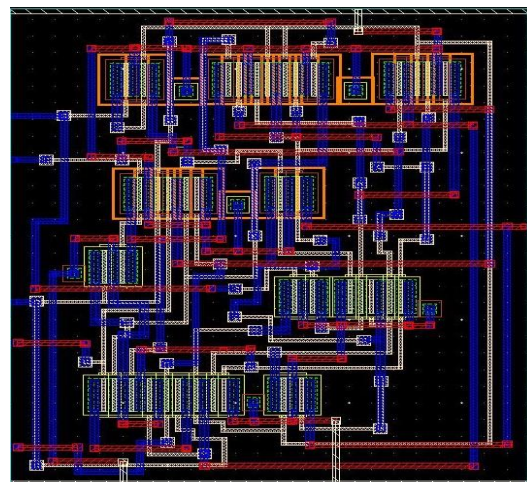


Fig.6: Layout with double via connection (after implementing all three methods).

## V. CONCLUSION

This research work carried out has been focused on optimizing the total layout area by reducing the unwanted white space present in the layout using 1) depletion sharing, 2) minimum distance rule and 3) different metal layers together. Reliability of the proposed layout has been taken care by using double vias in place of single vias wherever possible. Post simulation power calculation shows results that on reducing the area, power consumption is also reduced. If the above said methodologies are automated, it can be implemented for any industry standard projects which are developed on same platform.

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