MODIFIED SVPWM FED NINE SWITCH INVERTER FOR MOTOR LOAD

M. Nirmala, K. Baskaran, S. Sowmiya

Department of Electrical and Electronics Engineering, Kumaraguru College of Technology, Coimbatore, India.
nirmalalalithkumar25@gmail.com, sowmisiva4@gmail.com

ABSTRACT

The nine-switch inverter has been suggested in order to reduce the switching components and the cost of regular six switch inverter. In this paper, the conventional Space Vector Modulation (SVM) and Level-Shift Space Vector Pulse Width Modulation (SVPWM) design of nine-switch inverter is contemplated, controlling the two independent parallel ac induction motors without the shoot-through in the inverter leg. The SVPWM is proposed for minimizing total harmonic distortion (THD). The dual output voltages and phase currents can prevent the distorted attribute, which is originated by the crossover of the modulating signals. This will suitable for high power inverter application where cost and efficiency are vital decision factors. The mathematical models are suggested by the level shift SVPWM scheme and based on the zero-sequence injection principle. The offset control decrement are arranged by the interconnection of the modulation indices in level shift of the SVPWM modulating signals. The suggested modulation performance has been confirmed by the simulated implementation that is effectively carried out on the applicability of the proposed algorithm, the high modulation index is needed.

Keywords—NSI, SVPWM, level shift SVPWM, Induction motor, THD

I. INTRODUCTION

Inverters are used as dc/ac converter and power controller for ac load such as motor drivers. Independent control of two or more ac loads is requiring in many cases. The conventional solution is to use separate inverters. Due to this, the cost and volume of system will be increased. A dual output inverter has been using only nine semiconductor switches (see Fig. 1) in [1]. The Nine Switch Inverter (NSI) is composed of two inverters with three common switches [2, 3]. In nine-switch inverter, modulation index of two outputs are added, must be less than or equal to one. Accordingly, output of voltage amplitude is smaller, compared with two separate inverters [4]. In order to reduce total harmonic distortion (THD) and number of semiconductor switching devices, some definite switching patterns for SVM are proposed.

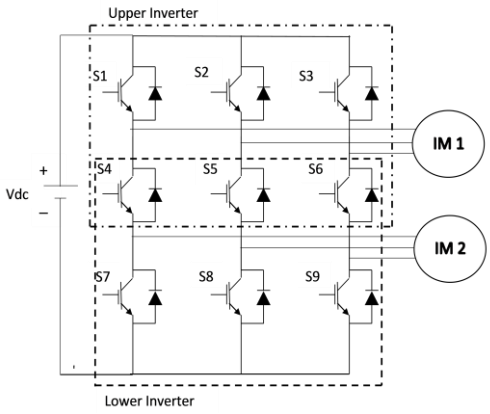

Fig. 1. Nine-switch inverter.

The control method nine switch inverter is shown in Fig.2. There are two reference signals (upper and lower) for each phase. The upper and lower reference signals are linked to upper and lower outputs. The gate signal of upper switch leg is generated by correlating the upper reference signal and carrier signal of the related phase (V_{refUJ}). Similarly, the gate signal of lower switch is achieved from the carrier signal and lower reference signal of the related phase (V_{refLJ}). The gate signal for mid switch is accomplished by the logical XOR gate signals for upper and lower switches. With this method, always two switches are ON in each leg.

For each switching, for both outputs there are six vectors cycle: two nonzero vectors, one zero vector (0 0 0), 2 non-zero vectors and 1 zero vector (1 1 1) {2 active short zero (0 0 0) 2 active long zero (1 1 1)}. In an active vector, output load is connected to the dc input source, while in a zero vector, the output load is short-circuited. Whenever the outputs has an active or short zero (0 0 0) vector, the other output has long zero (1 1 1) vector.

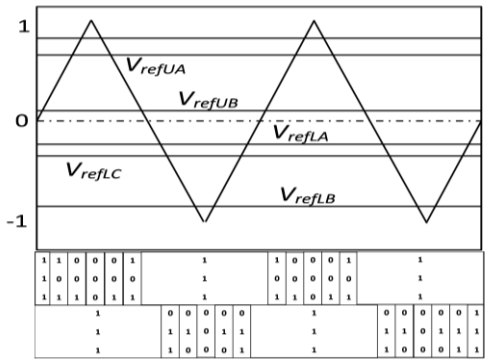

Fig. 2. *switching vector.*

This paper presents the level-shift space vector PWM (SVPWM) algorithm for controlling the nine-switch inverter. The proposed mathematical model, based on zero-sequence injection for simplicity, can eliminate the mentioned drawbacks and reduce the offset control, which is suitable for CF-mode without shifted phase of the modulating signal for the high modulation index requirement. Simulation results on demonstrate the feasibility of the proposed algorithm performance.

II. SPACE VECTOR PULSE WITH MODULATION

In regard to Fig. 2, there are three different semiconductors ON-OFF position in each leg. These position can be called (1), (0), and (−1), are illustrated in table I. J refers to leg A, B, C and U, M, L refers to upper, mid, and lower semiconductor, respectively.

A specific sequence was created by the combination of switching vector of both outputs as in Fig. 4. This

sequence is used to design SVM method. For each switching cycle consists of 12 vectors. In Table II the switching vectors are listed. The upper active vectors are V1 –V6. In these vectors, the upper output is in active state, and the lower output is in zero state. There is an inverse logic in lower active vectors (V_7 –V_{12}). In zero vectors (V_{13} –V_{15}), both outputs are in zero state.

All possible variations of switching states {1}, {0}, and {−1} are not included in Table II. Since a vector including {−1} and {0} connects both loads to the dc source at the same time, will lose the load independence and their frequencies become independent. This is the reason for avoiding a vector that includes combinations of {−1} and {0}.

In none of the switching vectors as listed in Table II, at the same time both outputs are not in an active. Yet, in vectors including both {−1} and {0} such as {−1, 1, 0}, both outputs are in active state. These vectors are neglected because there are not all combinations of active vectors for both outputs. For lower output this vectors (0 1 1), (0 0 1), and (1 0 1) are not available. Therefore, outputs cannot be controlled independently.

TABLE I. ON-OFF POSITION OF LEGS

	S_{JU}	S_{JM}	S_{JL}
1	ON	OFF	ON
0	OFF	ON	ON
-1	ON	ON	OFF

TABLE- II: SVM SWITCHING VECTORS

vector	Leg A	Leg B	Leg C	Type
1	1	0	0	Upper Active
2	1	1	0	
3	0	1	0	
4	0	1	1	
5	0	0	1	
6	1	0	1	
7	-1	1	1	Lower Active
8	-1	-1	1	
9	1	-1	1	
10	1	-1	-1	
11	1	1	-1	
12	-1	1	-1	
13	1	1	1	Zero
14	0	0	0	
15	-1	-1	-1	

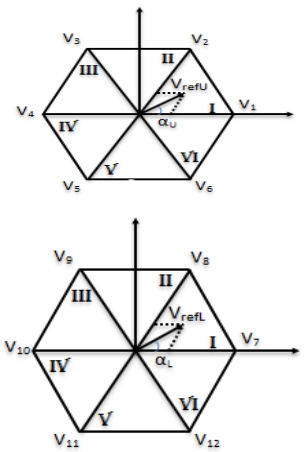

Fig. 3. *Space vector diagrams for nine-switch inverter. (a) Upper output. (b) Lower output*

To determine the proper active vectors, two space vector diagrams are purpose as shown in Fig. 5. The diagrams (a) and (b) are used to determine the upper and lower active vectors, respectively. The SVM active vectors are determined with concern to location of upper reference signal (V_{refU}) in the diagram (a) and lower reference signal (V_{refL}) in the diagram (b). For the upper and lower outputs the reference signals are defined as

$$\overline{V}_{refU} = V_{refU}\angle\alpha_U \quad (1)$$

$$\overline{V}_{refL} = V_{refL}\angle\alpha_L \quad (2)$$

Where

$$\alpha_U = 2\pi f_U t + \varphi_U \quad (3)$$

$$\alpha_L = 2\pi f_L t + \varphi_L \quad (4)$$

Where f_U, f_L are the frequencies, and Φ_U, Φ_L are the phases. All zero vectors V_{13}, V_{14}, V_{15} can be used for zero states. The type of zero vectors can be selected based on control goals and optimization such as minimum of semiconductor switching.

The switching time intervals for vectors are calculated as where the time interval of upper active vectors are T_1 and T2, time interval for lower active vectors are T_3 and T_4, time interval for zero vectors is T_0 and T is switching period. M_U and M_L are upper and lower modulation indices.

The time intervals of sum of active vector must be less or equals to T. Sum of modulation indices raises about 15%—a very important feature to provide higher torque for a given input dc-voltage.

This switching sequence is proposed to decrease the number of semiconductor switching. The zero vectors are placed just within two upper and lower active vectors. State {1} or {0} are upper active vectors and state {1} or {−1} are lower active vectors. If V_{13} zero vector is placed mid of the active vectors, minimum number of switching is required.

While if V_{14} or V_{15} zero vectors are used, number of switching is increased.

In a switching sequence there are two odd active vectors (V_1, V_3, V_5, V_8, V_{10}, and V_{12}) and two even active vectors (V_2, V_4, V_6, V_7, V_9, and V_{11}). Two legs are in state {1} in an even active vector, while only one leg is in state {1} in an odd active vector. If even active vectors are placed next to V_{13}, number of switching will be reduced even more.

There are other possible switch generation methods too, e.g., there is a switching method, to reduce THD. To minimize THD, active vectors for each output should be centrally placed within the switching period [5]. In a sequence, zero vectors are inserted between active vectors. V_{14} is inserted between upper active vectors and V_{15} is inserted between lower active vectors.

III. LEVEL SHIFT SPACE VECTOR PULSE WITH MODULATION

To satisfy this concept, the modulating signal of the nine-switch inverter can be generally classified into two reference voltages. Therefore, the proposed level-shift SVPWM algorithm is presented to avoid the crossover of the two reference voltages with the reduction of the offset control. The proposed modulation is based on the 'Zero-sequence injection' method by the addition of the

selective zero-sequence signal into the sinusoidal reference signal. The three phase reference voltages $v_{1,j}$ and $v_{2,k}$ for the dual SVPWM reference voltages can be expressed in terms of

$$V_{1,J} = M_1 sin(2\pi f_1 t + \theta_j + \emptyset_1) \quad (5)$$

$$V_{2,k} = M_2 sin(2\pi f_2 t + \theta_k + \emptyset_2) \quad (6)$$

where M_1, M_2 are the modulation indices, f1, f2 are the fundamental frequencies, φ_1, φ_2 are the phase shifted angles, and θj, θk are the phase angles (j and k belong to phase-to neutral voltages for A, B, C phases and U, V, W phases, respectively), from which θ_A, θ_U =0, θ_B, θ_V = $-2\pi/3$, and θ_C, θ_W =$2\pi/3$ radian. The selective zero-sequence voltages for the dual SVPWM reference voltages are given by

$$V^*_{1,0} = (\max(V_{1,j}) + \min(V_{1,j})) \div 2 \quad (7)$$

$$V^*_{2,0} = (\max(V_{2,k}) + \min(V_{2,k})) \div 2 \quad (8)$$

To achieve the SVPWM scheme for the nine-switch inverter, the three-phase sinusoidal reference voltages $V_{1,j}$ and $V_{2,k}$ are injected by the zero sequence voltage $v^*_{1,0}$ and $V^*_{2,0}$, respectively. The upper and lower SVPWM reference voltage. $V^*_{M1,j}$ and $v^*_{M2.k}$, enforcing the upper and lower inverters respectively, can be then generated by

$$V^*_{M1,J} = V_{1,j} - V^*_{1,0} + V_{offset\,1} \quad (9)$$

$$V^*_{M2,J} = V_{2,k} - V^*_{2,0} + V_{offset\,2} \quad (10)$$

Where the dc components are $v^*_{M1,j}$ and $v^*_{M2.k.}$ The above equations illustrate that the offsets $V_{offset1} = 1- M_1(\sqrt{3}/2)$ and $V_{offset2} = 1- M_2(\sqrt{3}/2)$ are found by controlling the peaks of $v^*_{M1,j}$ and $v^*_{M2.k.}$ for touching the uppermost and lowermost carrier peaks, respectively.

$$V'_{offset\,2} \geq (M_1 - M_2) \times (\sqrt{3}/2) \quad (11)$$

Since the lower inverter operates with the dominant load for $M_1 < M_2$, the lower SVPWM reference voltage is generated without the offset control. Therefore, the offset $V_{offset1}$ is rebuilt to $V'_{offset1,}$ that is

$$V'_{offset\,1} \geq (M_2 - M_1) \times (\sqrt{3}/2) \quad (12)$$

The crossover of dual SVPWM reference voltages that must be in phase for the high modulation index offer can be done by the offsets in (11) and (12).

$$V'_{offset\,1} \geq (M_1 + M_2) \times (\sqrt{3}/2) \quad (13)$$

Where I is 1 for but 2 for, equation (13) indices that the lower modulation index for the case of and can be calculated by and respectively. The relationship between the modulation index and the peak value of the fundamental output voltage for both upper and lower inverters can be obtained from all the equations by,

$$\hat{V}_{HA} = (M_1 V_{dc}) \times (\sqrt{3}/2) \quad (14)$$

From (14), the range of the modulation indices M_1 and M_2 for the linear modulation operation is expanded to the range of 0 to 1.15 by the zero-sequence injection method, from which the maximum magnitude of the fundamental line-to-line output voltage can be boosted by 15.5% that is higher than that of the sinusoidal PWM (SPWM) scheme.

Switching states and switch signal arrangements for leg *A* using the level-shift SVPWM scheme discussed previously with the modulation indices $M_1 = 0.6$ and $M_2 = 0.8$ for the case of $M_1 < M_2$ in CF-mode. The lower SVPWM reference voltage, $v^*_{M2,U}$, is vertically centered by without the offset control. Therefore, the upper SVPWM reference voltage, $v^*_{M1,A}$, is shifted vertically above the lower SVPWM reference voltage until touching with its counterpart. This leads to the twice points of touching per cycle as shown by the two dotted line squares. By zooming only one, the switches S_{HA}, S_{MA}, and S_{LA} are operated by State 3 for the switching states as Table I, where the switch signals controlling the switches S_{HA} , S_{MA} , and S_{LA} are generated by comparing only a carrier V_C with the dual SVPWM reference voltages.

When the upper SVPWM reference voltage is higher than the carrier, S_{HA} is switched on. Whereas S_{LA} is switched on due to the lower SVPWM reference voltage being lower than the carrier. For the switch S_{MA}, its switch signal is generated by exclusive or logical operation between the switch signals of S_{HA} and S_{LA}. However, this instance may lead to the short-through in an inverter leg feasibility. It can be solved by inserting the dead time to the switches in the nine-switch inverter. By the way, the dual SVPWM reference voltages possibly crossover each other. If this occurs, it will cause the distortion in the dual inverter output voltages, which is undesirable in most cases

IV. SIMULATION RESULTS

Nine switch inverter –the proposed level shift SVPWM techniques has been used to reduce the THD value below 10.the simulation results of SVPWM and the proposed level shift SVPWM based nine switch inverter are given below. Two independent induction motor are connected through RC filters are connected to the output of the inverter.

The output of the SVPWM and level shift SVPWM based nine switch inverter are listed below:

SVPWM output are: Vo(line)=100V , Vo(ph)=75V , speed=1460, THD=4.85%

Level Shift SVPWM OUTPUTS are: Vo(line)=440V, speed=1720rpm, THD=4.41%.

TABLE III: OUTPUT PARAMETERS FOR SIMULATION

Parameters	SVPWM	Level shift SVPWM
Vo (line)	100V	440V
Speed	1460rpm	1720rpm
THD	4.85%	4.41%

The Simulation Output of SVPWM NSI

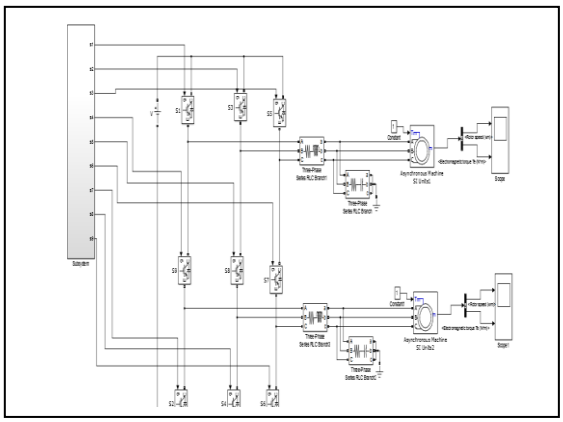

Fig. 4. Simulation Diagram of SVPWM NSI

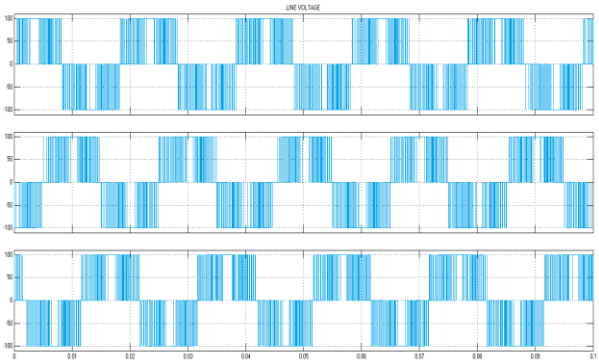

Fig. 5. Line Voltage of Inverter Output 1

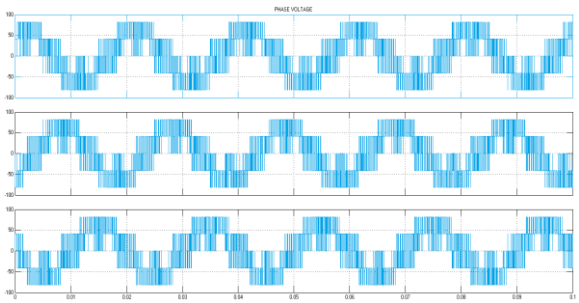

Fig. 6. Phase Voltage of Inverter Output 1

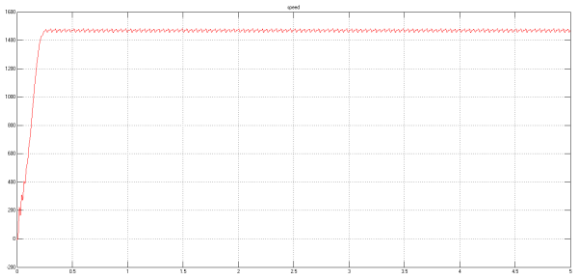

Fig. 7. Speed of the Induction Motor 1

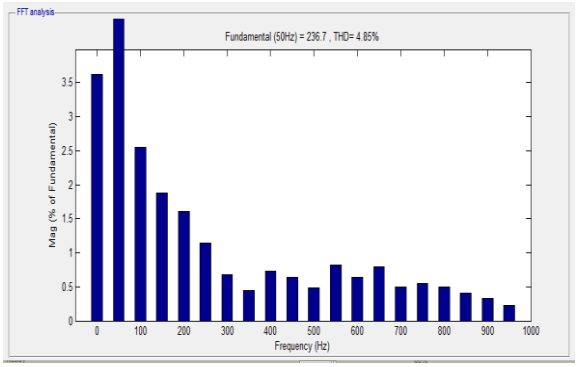

Fig. 8. FFT Analysis of output voltage SVPWM

The Simulation Output of Level Shift SVPWM

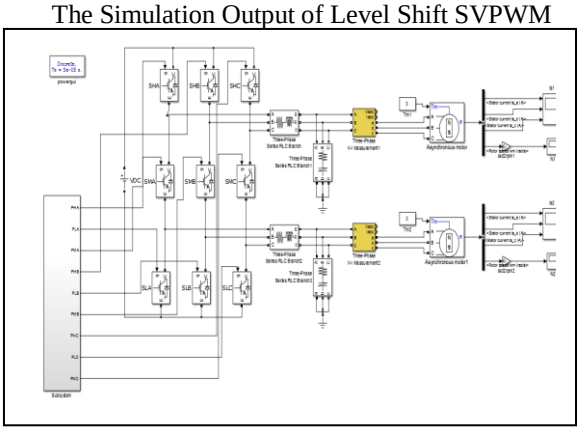

Fig. 9. Shows the Simulation Diagram of Level shift SVPWM

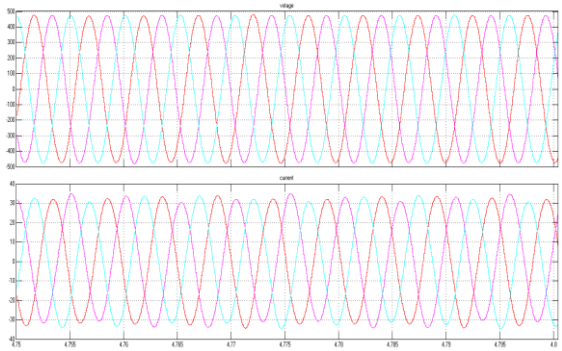

Fig. 10. Output voltage waveform of level shift SVPWM

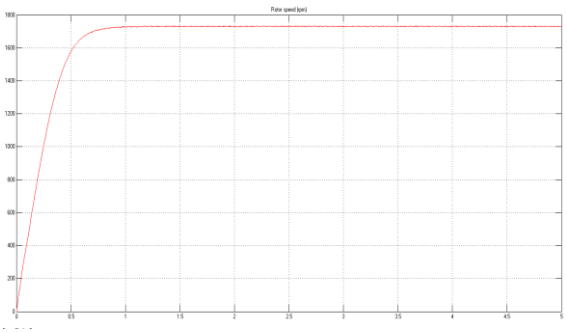

Fig. 11. Speed of the Induction Motor 1.

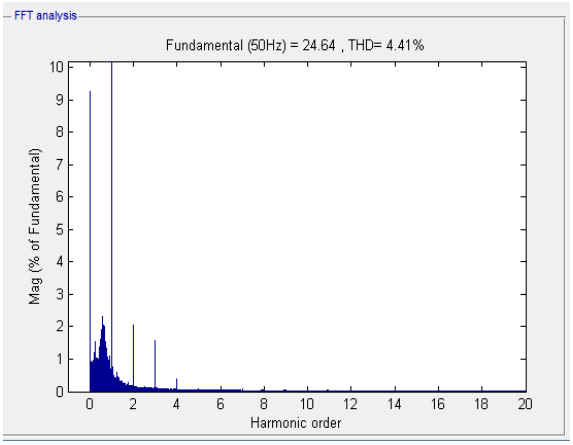

Fig. 12. FFT Analysis of output voltage Level Shift SVPWM

CONCLUSION

This paper presents the performance comparison of SVPWM and Level Shift SVPWM control for nine switch inverter driving two Induction motor load. For both methods, simulation has been carried out using matlab. The THD of the output voltage has been reduced to 4.41% in Level shift SVPWM technique. The simulation results have been obtained for both the methods. The THD of the output voltage using Level shift PWM is less when compared with SVPWM.

REFERENCES

[1] T. Kominami and Y. Fujimoto, A novel nine-switch inverter for inde-pendent control of two three-phase loads, Proc. IEEE Ind. Appl. Soc. Annu. Conf. (IAS), Pp. 2346–2350 (2007)

[2] C. Liu, B. Wu, N. Zargari, and D. Xu, A novel three-phase three-leg AC/AC converter using nine IGBTs. IEEE Trans. Power Electron. 24(5): 1151–1160 (2009).

[3] C. Liu, B. Wu, N. Zargari, and D. Xu, A novel nine-switch PWM rectifier-inverter topology for three-phase UPS applications. J. Eur. Power Electron. 19(2): 1–10 (2009)

[4] K. Oka, Y. Nozawa, R. Omata, K. Suzuki, A. Furuya, and K. Matsuse, Characteristic comparison between five-leg inverter and nine-switch in-verter, Proc. Power Convers. Conf., Nagoya Pp. 279–283 (2007)

[5] P. C. Loh, D. M. Vilathgamuwa, Y. S. Lai, and G. T. Chua, Pulse-with modulation of Z-source inverters. IEEE Trans. Power Electron. 20(6): 1346–1355 (2005)