A LOW POWER RECODING METHODOLOGY FOR THE DESIGN OF A MAC UNIT USING FUSED ARCHITECTURE

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ABSTRACT

The paper presents a new fused methodology proposed for the MAC unit in 65nm which consumes less power, area and reduces the critical path delay. This paper focuses on the efficient design of Fused adder-multiply operators, targeting the optimization of the recoding scheme for direct shaping of the Modified Booth form of the sum of two numbers. More specifically, we propose new technology advancement compared to the recoding technique available in 90nm technology. The proposed technology decreases the critical path delay and reduces the power consumption. The proposed technology not only reduces the power but area also been reduced. The work is done for different fused approach using conventional and signed-bit Adders as building blocks. The implementation is done using Spice models, results are observed and power analysis is made.

Index Terms— Low power, Recoding schemes, MAC unit, Fused Architecture, Modified Booth Algorithm.

I. INTRODUCTION

In today's consumer electronics Digital Signal Processing (DSP) plays a very important role and provides custom accelerators for products on multimedia, communications etc. The DSP applications perform large number of arithmetic operations as their implementation is based on computationally intensive kernels, such as Fast Fourier Transform (FFT), Discrete Cosine Transform (DCT), Finite Impulse Response (FIR) filters and signals' convolution. As expected, the performance of DSP systems is inherently affected by decisions on their design regarding the allocation and the architecture of arithmetic units. Recent research activities in the field of arithmetic optimization have shown that the design of arithmetic components combining operations which share data, can lead to significant performance improvements. One such performance improvement methodology is proposed in this project. The main elements like multi-plication, multiply-Accumulator (MAC) and Multiply-Add (MAD) units make efficient implement-tations of DSP algorithms compared to the conventional ones, which use only primitive resources .In literature several architectures have been proposed to optimize the performance of the MAC operation in terms of area occupation, critical path delay or power consumption.

Although the direct recoding of the sum of two numbers in Modified Booth(MB) form leads to a more efficient implementation of the fused Add-Multiply (FAM) unit compared to the conventional one, existing recoding schemes are based on complex manipulations in bit-level, which are implemented by dedicated circuits in gate-level. High data rates and more features in many hand held applications have increased the demand of high performance DSP based chipsets or system on chip devices which require arithmetic optimization in every design. The conventional devices designed for Multiply-Accumu-lator (MAC) and Multiply Add (MAD) units uses only primary resources which increases the power, area and slow in execution. As digital multiplication used extensively for conventional multipliers new algorithms were proposed in the literature. The existing design of the multiplier unit allocates an adder

and then driving its output to the input of a multiplier, increases significantly both area and critical path delay of the circuit.

Booth multiplication algorithm or Booth algorithm as an algorithm or method for multiplying binary numbers in two's complement notation is simple method but needs more attention. Modified booth algorithm played a vital role in previous generation processor cores. Now a day's extensive technology improvement have helped the resear-chers to come up with new modified booth algorithm. This helped in reduction of partial products. The proposed method optimize the design by fusion techniques based on the direct recoding of the sum of two numbers in its Modified Booth (MB) form. The rest of the paper is organized in this manner. In section 2 detail analysis of literature is done. In section 3 Background algorithm is explain-ned.The proposed methodology is presented in section 4 followed by result and discussion in section 5.

II. LITERATURE SURVEY

In Literature several algorithm is proposed for the designing the structure for high-speed multiplier circuit. Recently hybrid methods were also pro-posed like wave pipeline structures when array multipliers were still dominating the world of computing device. In their paper [1] Alexandru Amaricai et.al has proposed a dedicated Divide add fused architecture which performs the combined operation of floating-point (FP) division and addi-tion/subtraction. The fused design unit increases the accuracy and performance of applications where this combined operation is frequent, such as the interval Newton's method or the polynomial appro-ximation. The proposed DAF unit even though looks like FP multiply-accumulate units the divider is designed based on digit-recurrence algorithms. The design tradeoff is lesser latency for best cost. In [2] a fused floating point based FFT implementation is proposed based on two fused floating- point operations. The proposed operation is based on fusing two-term dot product and add-subtract unit. The work is further extended in the radix-2 and radix-4 butterflies' implementation efficiently with

the two fused floating-point operations. The paper proves that the fused FFT butterflies are about 15 percent faster and 30 percent smaller than a convenional implementation. Also the findings demonstrate the numerical results to be slightly more accurate through the usage of operations. Nikolaidis et al., [3] proposed a novel method for the accurate calculation of the transition activity at the nodes of multiplier-accumulator (MAC) architecture for finite impulse response filters. The transition activity per bit of a signal word is modeled according to the dual-bit-type (DBT) model. An efficient analytical method based on multiplexing in time of signal sequences with known statistics has been proposed for the determination of the signal statistics at each node of the MAC architecture. The paper presents the experiments carried out both with synthetic and real data and proves its efficiency. Nowadays compressors are widely been used for multiplier implementation. A 16-Bit by 16-Bit MAC is imple-mentted using Fast 5:3 Compressor cells. The cell is designed by applying two rows of fast 2-bit adder cells to five rows in a partial product matrix. The paper reports a 14.3% speed improvement in terms of XOR gate delay on the usage of compressor cell. For a dynamic CMOS circuit implementation using 0.225 μm bulk CMOS technology the reported speed improvement is 11.7% with 8.1% less power consumption. Young-Ho Seo et.al [4] proposed a new architecture of multiplier and accumulator (MAC) for high speed arithmetic. The overall per-formance was elevated b proposing a CSA tree using 1's-complement-based radix-2 modified Booth's algorithm (MBA) and a modified array for the sign extension. The proposed tree architecture propagates the carries to the least significant bits of the partial products and generates the least significant bits in advance to decrease the number of the input bits of the final adder. The inter-mediate results are accumulating in the type of sum and carry bits through pipeline through which performance is improved. The paper reports the experimental results of the proposed architecture in 250nm, 180nm, 130nm, and 90 nm standard CMOS library. Wen-Chang Yeh et.al [5] in their paper presented a novel split-radix fast Fourier transform (SRFFT) pipeline architecture design using mapping methodology. The latency between complex multi-plication and butterfly operation is balanced. The reported power consumption is reduced by an amount of 15%. A redundant arithmetic based FFT butterfly imple-menttation based on utilization of carry-save adders and a signed-digit representation of the multipliers in the multiplications is proposed in [6]. Other works based on sum-of- product (SOP) blocks [7], fast multiplier [8] is done. Marc Daumas et al., [9] proposed a booth multiplier accepting both a redundant and redundant input with no additional delay. Other multiplier design includes Left-to-Right Array Multiplier Design proposed by Zhijun Huang et al., [10] which is based on signal

flow optimization, left-to-right leapfrog (LRLF) signal flow, and splitting of the reduction array.

III. THEORETICAL BACKGROUND

An existing method is modified and proposed for a higher technology with lower power and area. In the existing method an Adder-Multiplier units are desi-gned and their inputs added then driven to multiplier .first driven to an adder and then the input and the sum are driven to a multiplier. This leads to addi-tional delay in the critical path. In addition to that the critical path lengthens based on the bit width. But using a Carry-Look-Ahead (CLA) adder may reduce the delay but the tradeoff is increase in area occupation and power dissipation. The proposed method is an optimized design of the alignment of adder and the MB encoding unit into a single data path block by direct recoding of the sum. The pro-posed method named Modified Fused Add-Multiply (MFAM) contains one adder at the end (final adder of the parallel multiplier). The proposed technology significant reduces the area and critical path delay.
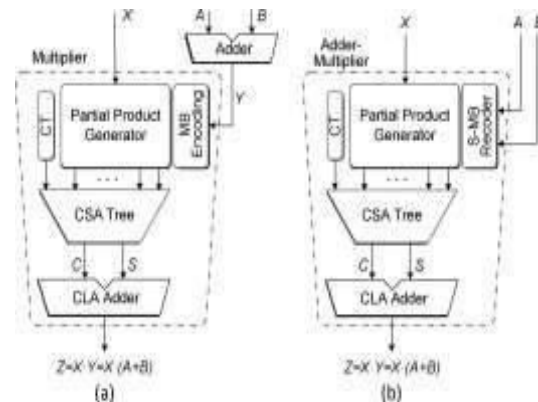

Fig.1. Add multiply operator based on the (a) conventional design and (b) fused design with direct recoding of the sum of A and B in its MB representation.

IV. PROPOSED SUM TO MODIFIED BOOTH RECODING TECHNIQUE

The add-multiply blocks (MAC& MAD) form the major building blocks of all DSP processor core. When conventional methods use direct and recoding schemes still more schemes are required for specific propose processor. In this paper we propose a fused add multiply architecture. This optimizes the recoding scheme and reduces the critical path delay and power consumption. The proposed architecture which is the adoption of work by Kostas Tsoumanis et al., [11] not only reduces the critical path and power but most importantly area. The proposed schemes are easily applied to signed or unsigned numbers (odd and even number of bits). The inputs are in 2's compliment form and in transformed using recoding cell to get the MB bits. The three recoding schemes are shown in figure.3-5.

V. RESULT AND DISCUSSION

The new fused methodology is implemented for the MAC unit in 65nm Predictive technology models using Spice tool. The power analysis is done and tabulated in table 1. From the observation it is found that the proposed method consumes less power, area and reduces the critical path delay. This efficient design of

Fused adder-multiply operators, targeting the optimiza-tion of the recoding scheme for direct shaping of the Modified Booth form of the sum of two numbers works with voltage 1V.

TABLE I. TABLE TYPE STYLES

S.No	Circuit	Power in (fW)
1	MB encoder	10.3793607863
2	MB multiplier	43.733389891
3	HA*	7.0848898631
4	HA**	7.04919664807
5	FA*	7.08480043163
6	FA**	7.08480043163
7	S-MB1 even	0.01287807501
8	S-MB1 odd	0.00676094363
9	S-MB2 even	46.6622302136
10	S-MB2 odd	0.03763458086
11	S-MB3 even	93.3134887617
12	S-MB3 odd	163.792854682

VI. CONCLUSION

In this paper a new MAC unit is been designed and implemented using fused technique. The work focu-ses on optimizing the design of the Fused-Add Multiply (FAM) operator. The work uses a structured technique for the direct recoding of the sum of two numbers to its Modified Booth form. Even though there are several MAC designs in the literature here in this project three different design methodology for the S-MB recoders is presented. The design is implemented and the power analysis is made for all the different type of recoding. In future the proposed methodology will be tested with real time data. The complete MAC unit will be designed using different architecture and the performance will be tested.

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