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A NOVEL CIRCUIT METHODOLOGY TO IMPROVE THE TRANSITION DELAY AND PROVIDE SIGNAL FEED THROUGH FOR INPUT DATA IN PULSE TRIGGERED FLIP FLOP

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ABSTRACT

In this paper, a new method to improve the transition delay, Conditional Pulse enhancement and reduction in transistor count for Flip Flop is proposed which consumes less power and area. The design featuring an explicit type pulse-triggered structure improves the problem arises due to transition delay. The clocked Pseudo NMOS style structure enhances the efficiency and reduces the load capacitance. The design which successfully solves the long discharging path problem also reduces the transistor count in the discharge path. The Proposed circuit is implemented using Predictive technology Model in CMOS 90-nm technology. The proposed design outperforms the existing method by reducing the power by 15% and 40% with two existing methods.

Index Terms— Flip-flop (FF), low power, pulse-triggered, Transition Delay, Conditional Pulse enhancement

I. INTRODUCTION

Memory Devices are getting developed day by day in different applications. New technology has allowed the chip to be so small and to consume less power. In literature several methods are available which improves the design and consume lesser power. Kawaguchi et al., [1] proposed a reduced clock-swing flip-flop (RCSFF which is composed of a reduced swing clock driver and can reduce the clock system power of a VLSI down to one-third compared to the conventional flip-flop. The RCSFF can also reduce the RC delay of a long RC interconnect to one-half. Partovi et al., [2] presented a hybrid latch-flipflop (HLFF) timing methodology for substantial reduction in latch latency and clock load. Klass et al., [3] presented a method to reduce the pipeline overhead; a new family of edge-triggered flip-flops has been developed. The flip-flops belong to a class of semidynamic and dynamic circuits that can interface to both static and dynamic circuits. Stojanovic et al., [4] in their paper, proposed a set of rules for consistent estimation of the real performance and power features of the flip-flop and master–slave latch structures. Flip-flops and latches are crucial elements of a design from both a delay and energy standpoint. Tschanz et al., [5] compared several styles of single edge-triggered flip-flops, including semidynamic and static with both implicit and explicit pulse generation. They presented an implicit-pulsed, semidynamic flip-flop (ip-DCO) which has the fastest delay of any flip-flop considered, along with a large amount of negative setup time.

Naffziger et al., [6] proposed tightly coupling micro-architecture choices to innovative circuit designs and the capabilities of the transistors and wires in the 0.18-µm bulk. Sadrossadat et al., [7] in this paper, proposed a method to achieve a high yield, while meeting the performance, leakage power, switching power, and layout area design specifications. The transmission gate-based master-slave flip-flop is selected as a design case study in their paper; however, the proposed framework is applicable to any other flip-flop circuit in the nanometer regime. Alioto et al., [8] proposed a methodology permits to optimize FFs under constraints within. In the paper [9] the influence of the clock slope on the speed of various classes of flip-flops (FFs) and on. the overall energy dissipation of both FFs and clock domain buffers is addressed. Analysis shows that an optimum clock slope exists, which minimizes the energy spent in a clock domain. Alioto et al., [10-11] has done an extensive comparison of existing flip-flop (FF) classes and topologies are carried out. Kong et al., [12] proposed a differential flip-flop which achieves power savings of up to 61% with no impact on latency while the single-ended structure provides the maximum power savings of around 67%, as compared to conventional flip-flops. Nedovic et al., [13] designed a new dual edge-triggered flip-flop that saves power by inhibiting transitions of the nodes that are not used to change the state is presented. Zhao et al., [14] in their paper, high-performance flip-flops are analyzed and classified into two categories: the conditional precharge and the conditional capture technologies. A new flip-flop is proposed named conditional discharge flip-flop (CDFF). Phyu et al., [15] proposed a new static dual edge-triggered flip-flop that incorporates no precharging and conditional discharging to efficiently reduce the switching activity at the internal node. Hwang et.al [16] Reported a novel low-power pulse-triggered flip-flop (FF) design where the pulse generation control logic, an AND function, is removed from the critical path to facilitate a faster discharge operation. A simple two-transistor AND gate design is used to reduce the circuit complexity. Rasouli et al., [17] proposed a new low-power flip-flops which are faster compared to previously proposed structures. The single-edge-triggered flip-flop, called the MHLFF (modified hybrid latch flip-flop), reduces the power dissipation of the HLFF (hybrid latch flip-flop) by avoiding unnecessary node transitions.

II. BACKGROUND METHODOLOGY

Pulse triggered Flip Flop are of implicit and explicit type. The two types of P-FF face one important problem. The transistors of pulse generators used in the P-FF normally vary in their W/L ratio and are often enlarged. So it can generate pulses of wider ON period to trigger the data capturing of the latch.

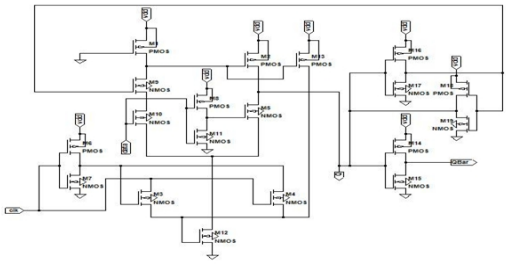

Figure 1. P-FF Design with Pulse Control Scheme

The problem increases when one pulse generator is shared among several blocks. This issue is investigated and rectified using conditional pulse-enhancement scheme proposed by Hwang et al., [16] given in figure 1. The other issue present in the P-FF design is the delay discrepancy in latching data "1" and "0". Jin-Fa Lin [18] proposed a method to speedup the data transition by shorte-ning the longer delay .This is achieved by feeding the input directly to an internal node of the latch given in figure 2.

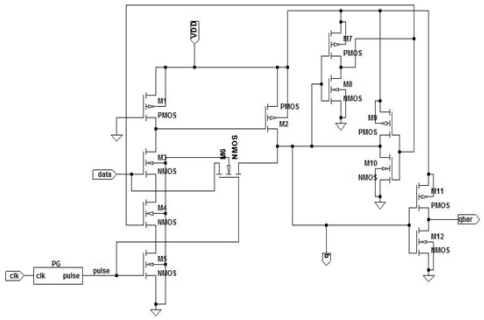

Figure 2. P-FF Design with Signal Feed-Through Scheme

III. Proposed P-FF Design

In this work a low-power flip-flop (FF) design is proposed (Figure 3) featuring an explicit type pulse-triggered structure based on conditional pulse enhancement and signal feed-through scheme. The proposed design distinct from the previous two methods proposed separately for delay reduction and power reduction. Three important problems are available in the existing circuits of the P-FF, first charge deficiency at nodes, more number of transistors in the discharging path and third one is the delay constraint. The proposed design with three structures in the circuit overcomes the problems associated with existing P-FF designs. The first one is a pseudo-nMOS logic style structure is designed using a weak pull-up pMOS transistor P1 with gate connected to the ground. P1 keeps the charge in the internal node connecting between the first stage and second stage. The load capacitance is also reduced by this method. Secondly the number of transistors stacked in the discharge path is reduced. Thirdly a pass transistor N5 is controlled by a pulse clock which enables the input data to drive the output node of the latch directly. The N5 along with P2 reduces the delay in transition by allowing a extra passage facility. N5 loading effect is negligible since it turns ON for a very less time.

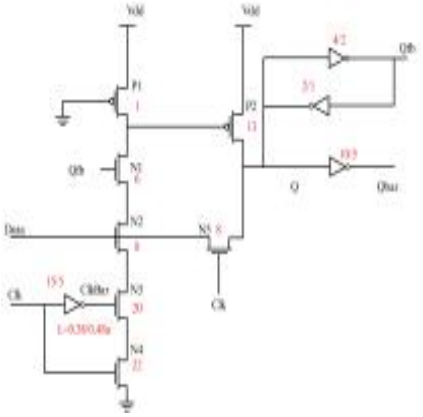

Figure 3. Proposed P-FF designs with Pulse Control Scheme and signal feed-through scheme

IV. Result and discussion

Figure 4. Implementation of Proposed P-FF designs with Pulse Control Scheme and signal feed-through scheme The conventional and proposed circuit (Figure 4 and 5) are implemented using Spice models in 90nm predictive technology Model and waveforms are observed. The performance of the proposed P-FF design is evaluated against existing designs through post-layout simulations.

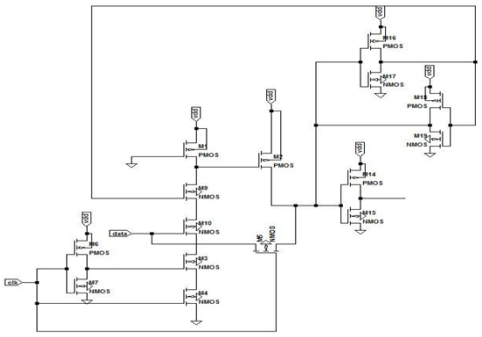

Figure 4. Implementation of Proposed P-FF designs with Pulse Control Scheme and signal feed-through scheme

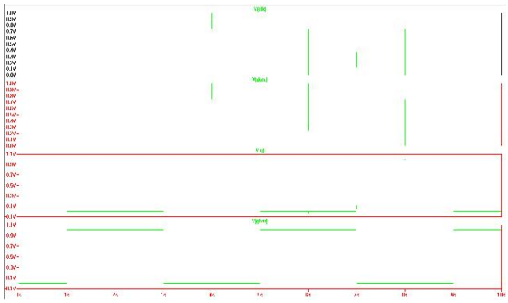

Figure 5. Output waveforms of Proposed P-FF designs with Pulse Control Scheme and signal feed-through scheme

TABLE I. PERFORMANCE COMPARISON OF VARIOUS METHODS

Method	Number of Transistor	Principle	Power Dissipation in (nW)
SCCER	17	Conventional Pulse triggered FF	682.28606
SCCER PULSE CONTROL SCHEME	19	Pulse Control Scheme	899.32445
Signal Feed Through Scheme (Static-CDFF)	24	Signal Feed Through Scheme	96.750966
Proposed Scheme	15	Pulse Control and Signal Feed-Through Scheme	587.89607

V. CONCLUSION

The issues in the pulse triggered FF is investigated and rectified in this work .A new method to improve the transition delay, Conditional Pulse enhancement and reduction in transistor count for Flip Flop is proposed. The explicit type pulse-triggered structure design consumes less power and area. The signal feed through block reduces the transition delay and enhances the efficiency and reduces the load capacitance.

VI. COPYRIGHT FORMS

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