

## DESIGN AND ANALYSIS OF CYCLIC REDUNDANCY CHECK USING QUANTUM-DOT CELLULAR AUTOMATA (QCA)

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### ABSTRACT

For communication systems, error detectors are required to make sure that error free signal is passed while transmitting/receiving. This error detection is resolved by a basic parity generator and parity checker in QCA. But these parity checkers cannot detect all forms of error. It checks whether it is an odd or even parity. To overcome the limits of parity checker, cyclic redundancy check (CRC) will be analysed and can be designed using QCA. Currently, QCA stands as a promising replacement for CMOS technology. In QCA, the operation is directed by the electron's position. The consumption of power in QCA is less and the operation of clock frequency is high over traditional CMOS. Also with technology reaching Nano-scale, CMOS does not function perfectly. CRC's are especially useful in digital circuits such as phase detectors, code converters and error detection & correction circuits. In this paper, QCA Designer tool ver. 2.0.3 has been used for the simulation of the design.

*Index Terms:* Communication, Error Detection, XOR/ XNOR, Information, Parity Generator, Parity Checker, QCA, Transmission.

### I. INTRODUCTION

Quantum-dot Cellular Automata (QCA) stands as a recent trend in lieu of quantum computation in nanotechnology with great prospective for dense memory, high operating frequencies and low power logic. Instead of transistors, silicon, and Complementary Metal Oxide Semiconductor (CMOS) technology, we can alternatively use QCA to eliminate high operating frequency [1]. In previous technology, it uses charge movement for producing current to transmit signals and execute operations [2]. QCA uses Coulomb force of electrons as their driving force [2]. Assumed clock pattern modulates an obstruction flanked by cells. This elementary cell to cell coalition is gratifying to endure a versatile figuring stratagem with very slight dissipation of power [3, 4]. More complicated circuits and a hulking scale fabrication of those circuits will need additional time, but the Nanoscale campaigns are vital to run into density, power, speed, performance disputes [5]. Recently, an innovative QCA adder model has shown that a decreased number of QCA cells. It also achieves a fast switching speed, very high density at room temperature. It has gained ample popularity in instigating which ever logical functionality [6]. QCA motion is circulated by the charge locus and no current or voltage drifts in consort with the cells. Several logical and functional circuits can be realized by using AND, OR, NOT, XOR/XNOR gates [7]. The XOR gate has gained a significant module in voluminous solicitations like code converters as well as pseudo-code generators [8]. Currently, scholars are centring on upgrading Nano-devices to detect/check errors in communication. A 3-bit odd and even parity generator coupled with checker technique had designed on the XOR gate using QCA nanotechnology to detect and check errors during broadcast. It also is used in reliable data

transmission over telecommunication networks. It also provides less area, clock delays and circuit complexity. Moreover, the proposed design (CRC) includes a better choice of error detection [9].

### II. QCA FUNDAMENTALS

#### A. QCA Cell

A QCA remains a set of four fixed dots called cell. These dots are arranged to form a square. Cells are used for a bi-stable charge configuration to denote information. One form of charge configuration embodies a binary "0" and other as "1". No current drifts in and out from the cell. Hence, QCA has a reduced amount of power dissipation than CMOS.

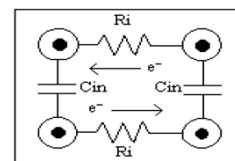


Fig. 1 QCA Cell model

The electrons are diagonally residing to each other. Cell in QCA is comprised of a twofold series linked metal dots divided by tunnelling resistance as well as capacitance, as shown in figure. 1. Where " $R_i$ " denotes the tunnelling resistance and " $C_{in}$ " denotes the internal capacitance.

#### B. Polarisation of QCA Cell

The state of electrons at a QCA Cell concludes its polarization and in turn directs the logical value of a signal diffusing over the sketch. The logic 0 signifies polarity '-1' and logic 1 signifies polarity '+1' respectively. The dualistic electrons are always residing in a diagonal locus owing to the occurrence of electrostatic

repulsive vigoursand wiced between them, as revealed in Figure.2

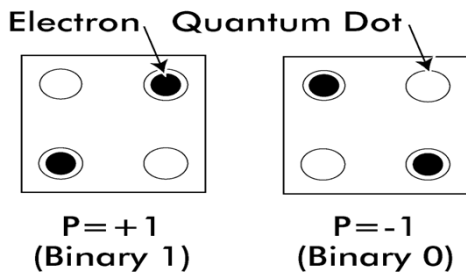


Fig.2 polarisation of QCA Cell

C. QCA Clock

In CMOS technology, the clock takes merely two situations (as small and a high). The clocking scheme used in QCA holds four stages explicitly switch ( from high to low), hold (low), release ( from small to high) and then relax (high). Devouring a phase variance of 90° to each other. **Figure 3** spectacles the clock stages in QCA. **Figure 4** displays the four existing clock signalsscheming QCA circuits. Every single signal is a phase differed by 90°. This maintains a harmonization in the circuit by controlling the potential intrusions among adjoining quantum-dots.

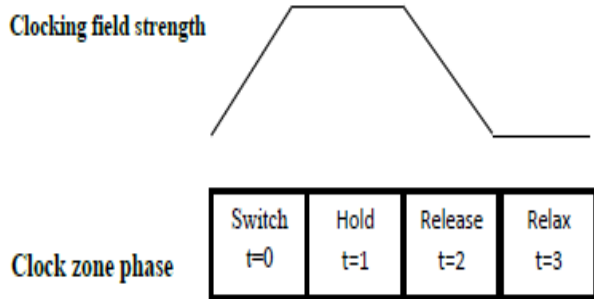


Fig. 3 QCA clock phases

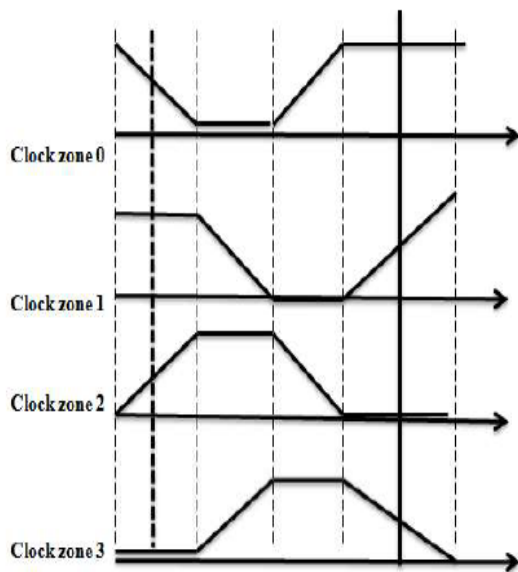


Fig. 4Four clock zones leading QCA

D. Wire placements in a QCA

QCA wire comprises of cable of cells and the cells stand related as unique by unique. QCA wire crossing is cast-off to diffuse signals commencing from one dot to another on a path. Logical values are conceded on or after cell to cell owing towards the Coulomb coalitions. There are dual types of placements (crossing) wire in QCA i.e. The Propagation of 90° QCA cross wire(Binary wire) in addition to 45° QCA wire (Inverter chain), as given away in Figure. 5 (a) and in Figure 5(b) correspondingly. 90° Wire conveys a sign with identical polarity as of one location to another; however, Inverter cable up turns the polarization of an in ward cell while abnormal quantities of cells remain sourced to it. Consequently, interconnect must be set to route without overlapping either horizontally and vertically to one another.

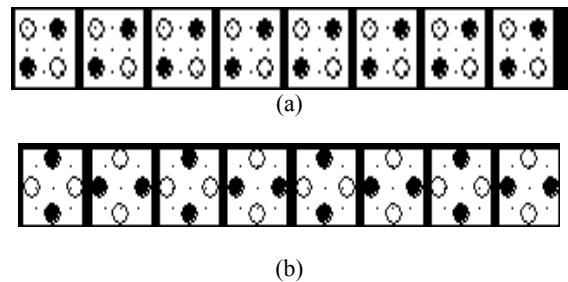
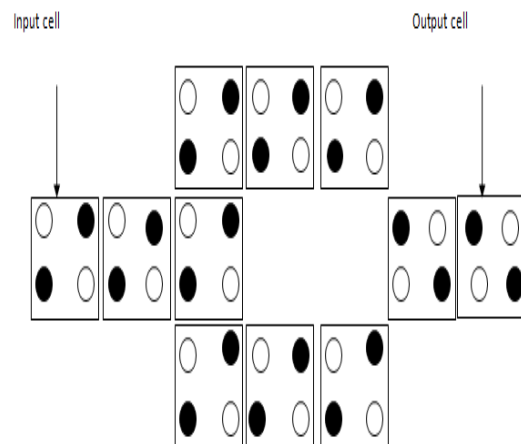


Fig. 5(a) 90°QCA wire crossover;(b) 45° QCA wire crossover

E. Basic gate utilization

There are dualbasic gate arrangements in QCA specifically theNOT gateand then Majority gate such as presented in the Figure 6(a, b). The Inverter gate performs as a NOT gate which bounces the upturnedoutgoing for the incoming. The Majority gate is real as a three terminal input gate. Further its output isemphasis to be the majority of contribution signals viz. From three inputs, double inputs stand at logic 1 and single input at logic 0, and thenoutput determines the logic 1. The Inverter gate endeavour as a NOT gate although the majority gate canenact as anAND/OR gate contingentin the direction ofimmobileseparationsmeared by one of its input.



(a)

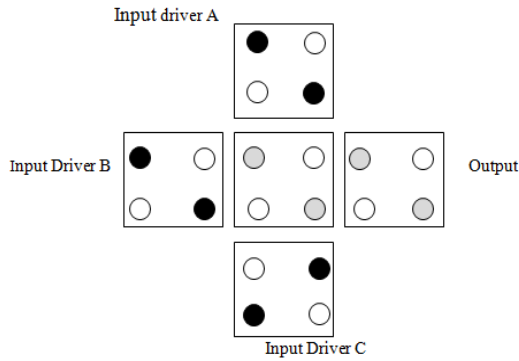


Fig. 6(a) Primary Inverter gate; (b) Fundamental Majority gate

### III. THE CRC IMPLEMENTATION

#### A. PARITY

Parity checking is a trouble-free custom of examining errors in data transmission. The sender totalities the bits of a message and then combines the bit to the message. This added bit is called as a parity bit. Then, receiver recurrences the math and equatesbits [10]. If bitsbe unlike, an error is detected. For example: 100 and 010 are same in parity, the original signal and a receiving signal are of same parity but both are different. This error in the signal is not identified using parity checker. Hence, there is need to have a higher level error detection mechanism. As a result, CRC is chosen to design in QCA.

#### B. THE PROPOSED CRC METHOD

The CRC is the scheme of identifying errors in digital data, but not for renderingrectification when errors are identified. It is used primarily in communication (digital networks) and in storage devices to identifyunintentional changes to uncooked data. Chunks of bitsincoming to the system gets a quick check value appended, based on the residue of a polynomial division of their contents. On retrieval the computation is repeated (encrypted word is repetively shifted(rotated), the significance is a new code word)and counteractive actions can be seized against recognized data corruption if it does not tally. The CRC is formed on polynomial arithmetic. Based on polynomial codes it can simply be realized usingShift register circuit and XOR gate [11, 9]. Figure 7 displays the block diagram of a polynomial equation  $X^5+X^3+X^1+X^0$  to perform CRC.

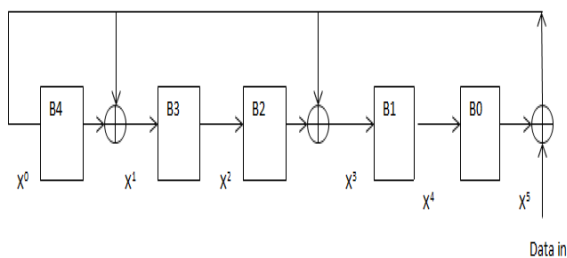
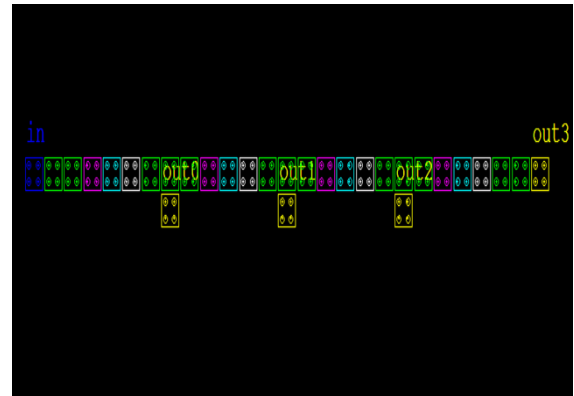


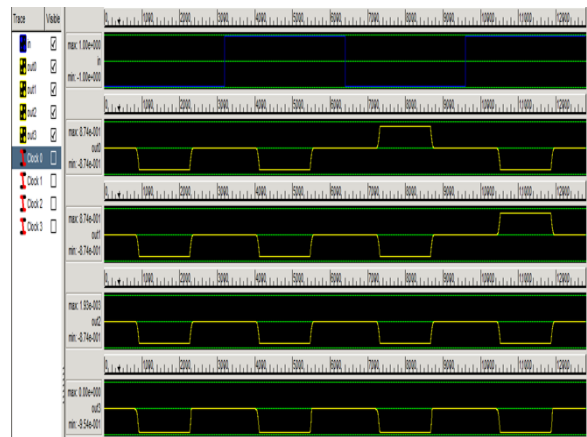
Fig. 7 Block diagram of  $X^5+X^3+X^1+X^0$

#### C. SHIFT REGISTER DESIGN

The input sequence is loaded to the shift register. It then shifts(rotates) continually to produce shifted output. Figure 8(a) spectacles the layout of shift registers. Figure 8(b) portrays the simulation result. The route is achieved with anidentical layer of 60° cells. The designcomprises of area 0.03 um<sup>2</sup>and density of cells in a circuit is 30.



(a)

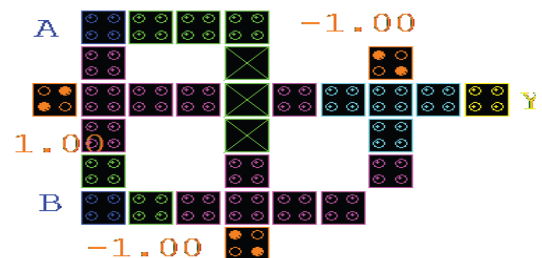


(b)

Fig. 8 (a)Shift registers outline;(b) Simulation result

#### D. XOR LAYOUT DESIGN

The layout of XOR gate design is revealed in Figure 9(a). Figure 9(b) illustrates the simulation outcome of the projected design. The homogeneous layer of the circuit is 90° cells. The circuit comprises of a lesser amount of area 0.03 um<sup>2</sup> and complexity of theircircuit is 30 cells.



(a)

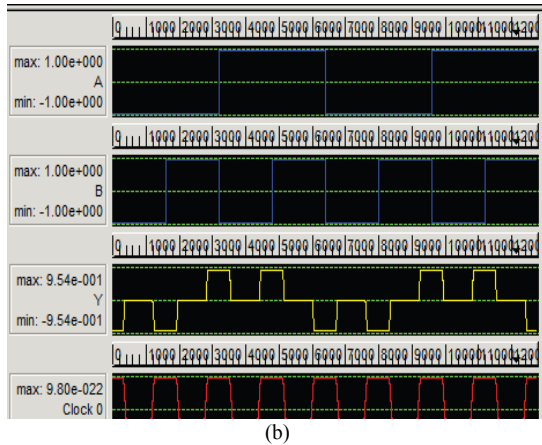
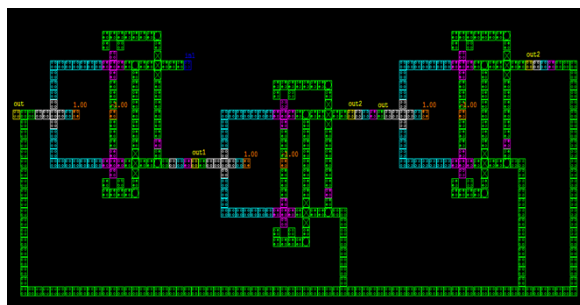


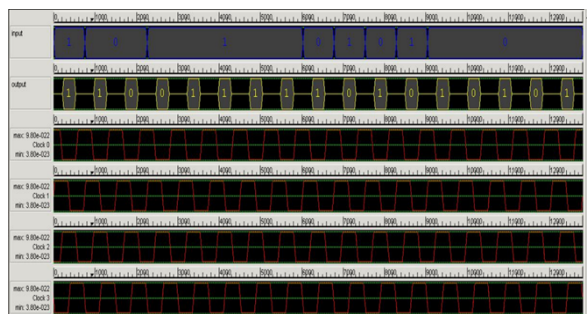
Fig. 9 (a) XOR gate outflow; (b) simulation results for XOR

### E. CRC LAYOUT DESIGN

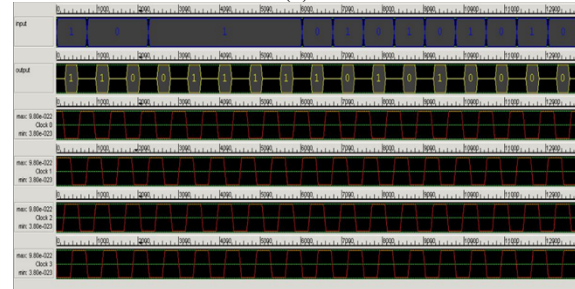
The input sequence is loaded with CRC bits which perform shifting and XOR operations as depicts in figure 10(a). Figure 10(b) provides a simulated output with CRC bit. The last four bits are CRC bits which are then fed back as an input to get final CRC output as portrays in figure 10(c). Then the given input and resulted output are analysed for identifying any errors.



(a)



(b)



(c)

Fig. 10 (a) CRC design flow; (b,c) simulation results

Layout of CRC design is revealed in Figure 10(a). The circuit consists of area 0.82  $\mu\text{m}^2$ . Figure 10(b, c) illustrates the simulated output of the CRC design.

### IV. CONCLUSION

The proposed design (CRC) provides the better error detection than parity. Parity checking cannot detect all forms of errors. It can detect an error (either odd or even quantities of ones and zeros) in 1 bit in a byte of data, but not 2, so some errors cannot be detected. Henceforth, the higher-level error detection mechanism (CRC) is designed by using a QCA. QCA presents a smaller amount of power dissipation and minimal area. QCA designer tool has been used for design and simulation. This can be efficiently used for data transmission.

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