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A NOVEL IMPLEMENTATION OF HIGH SPEED MULTIPLIER USING BRENT KUNG CARRY SELECT ADDER

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ABSTRACT

Multiplication is one of the most significant operations in every computational system and a multiplier forms the core of systems such as digital signal processing, image processing and microprocessor. Multiplier is an important element which contributes to the major power consumption in any system. Hence a fast energy efficient multiplier is always needed in electronics industry for fast computation of results. Recent applications of multipliers with various data lengths are always required in VLSI from processors to application specific integrated circuits (ASICs). In this work the designs of two different array multipliers is presented, one by using Ripple Carry Adder(RCA) based Carry Select Adder (CSLA) and Binary to Excess-1 Converter (BEC) based RCA CSLA for addition of partial product terms and the results are compared with the proposed multiplier using Brent Kung (BK) CSLA in partial product lines. The designs are synthesized using Quartus II Software. This design will meet the challenging task in modern VLSI design with respect to area and delay.

Index Terms— Ripple Carry Adder, Carry Select Adder, Binary to Excess-1 Converter, Brent Kung Adder.

I. INTRODUCTION

In most digital signal processing (DSP) systems, a multiplier is one of the key hardware blocks. Multiplier plays an important role in DSP applications like digital filtering, digital communications and spectral analysis. Power dissipation becomes one of the primary design constraints in DSP applications of portable, battery-operated systems. Since multipliers include complex circuits and must typically operate at a high system clock rate, the delay of a multiplier must be reduced in order to satisfy the overall design.

The simplest way to perform a multiplication is by using a single two input adder. For M and N bits wide inputs, the multiplication includes M cycles, using an N-bit adder. Multi-plication by shift and add algorithm adds together M partial products. The partial product term is generated by multiplying the multiplicand with the multiplier bit which, essentially is an AND operation and by shifting the result based on the multiplier's position. Similar to the familiar long hand decimal multiplication, binary multiplication involves the addition of shifted bits of the multiplicand based on the value and position of each of the multiplier bits. Thus, performing binary multiplication is much simpler than decimal multi-plication. The value of the binary digit can either be 0 or 1, thus, depending on the value of the multiplier bit, the partial products can either be a copy of the multiplicand, or 0- In digital logic, this is simply an AND function.

A faster way to implement multiplication is to resort to an approach similar to computing a manual multiplication. The entire partial product terms are generated simultaneously and organized in an array. The multioperand addition is performed to compute the final product. The resulting structure is called an array multiplier and based on three functions: partial product generation, partial product accumulation and final addition. The details of existing Multiplier Architectures are discussed in section II and the implementtation of proposed system is described in section III. The performance comparison and simulation result is presented and discussed in section IV and section V and VI gives the conclusion and limitation respectively.

II. EXISTING MULTIPLIER ARCHITECTURES

A. Multiplier using Ripple Carry Adder Based Carry Select Adder

The design of Carry select adder using Ripple Carry Adder is the conventional approach available but delay and area consumption is more. This CSLA generally consists of three RCAs and a Multiplexer. Addition of two n-bit numbers using a carry select adder is done with RCAs. One RCA is used for computing the summation of first 4 bits. In order to perform the calculation twice, once with the assumption of the carry being zero (Cin=0) and the other assuming one (Cin=1). Fig.1.shows the block diagram of RCA Based CSLA.

The 8x8 Multiplier comprises of 4, 4x4 multiplier sub blocks. Here, the multiplicands are having the bit size of (n=8) whereas, the result is of 16 bit in size. The input is broken in to smaller groups of size of n/2 = 4, for both inputs, that is a and b. These newly formed groups of 4 bits are given as input to 4x4 multiplier blocks and the result produced 8 bits, which are the output produced from 4x4 multiplier block are sent for addition to an RCA based CSLA.

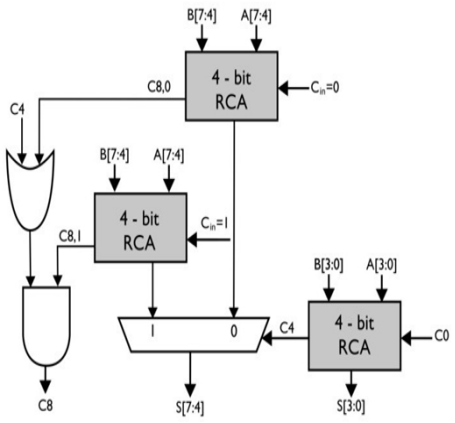

Fig.1. 8-bit Ripple Carry Adder based CSLA

Fig.2. shows the block diagram of 8 bit multiplier using RCA Based CSLA. Fig.3. shows the simulation result of Multiplier using Ripple Carry adder based CSLA.

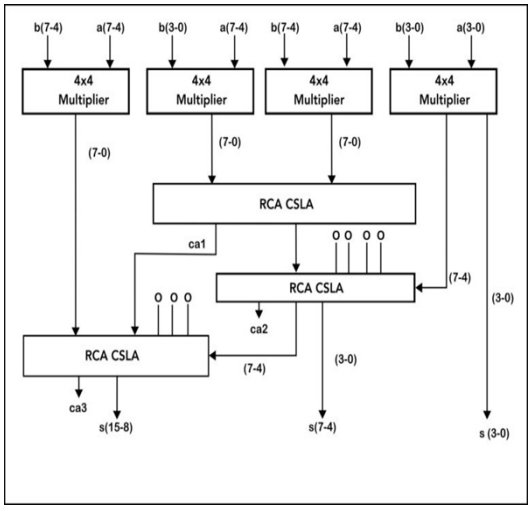

Fig.-2: 8-bit RCA based CSLA Multiplier

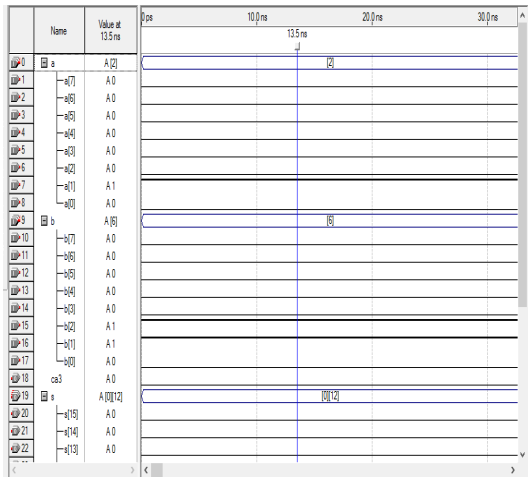

Fig.-3: Simulation result of RCA Based CSLA Multiplier

B. Multiplier Using Binary to Excess-1 Converter Based Ripple Carry Adder Carry Select Adder

The BEC based CSLA involves less number of logic resources than the conventional CSLA. The RCA for computing Cin =1 is replaced by BEC unit. BEC is used to add 1 to the input numbers. Less number of logic gates is used to design BEC and thus consumes less area than RCA. Hence area is reduced. Fig.4. shows the diagram of 4-bit Binary to Excess-1 Converter. Fig.5. shows the block diagram of Binary to Excess-1 based RCA CSLA.

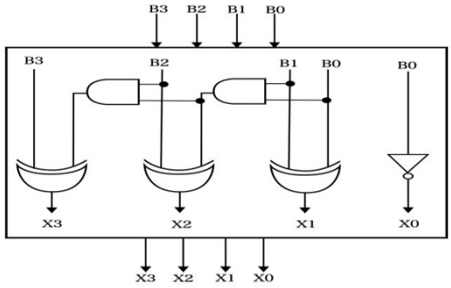

Fig.-4: Binary to Excess-1 Converter

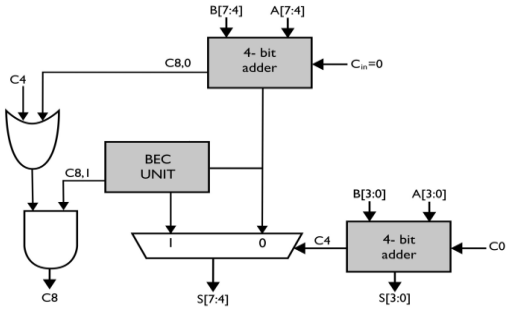

Fig.-5: 8-bit Binary to Excess-1 Converter based CSLA

The above obtained BEC based RCA CSLA is used for addition of the 8 bits that are coming from the 4x4 multiplier sub blocks. There are three adders needed for the partial product addition and final addition of bits. Finally the 16 bits give the multiplication of the two 8 bits input. Fig.6 shows the block diagram of 8-bit BEC Based RCA CSLA Multiplier.

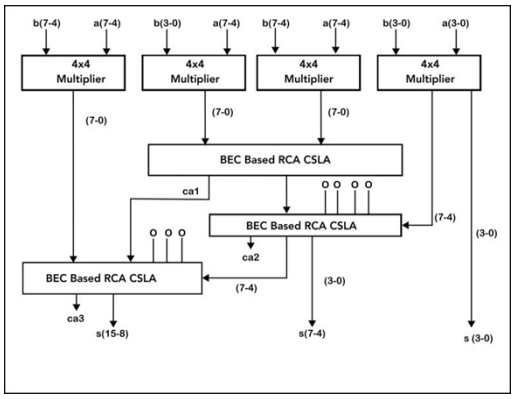

Fig.-6. 8-bit BEC Based RCA CSLA Multiplier

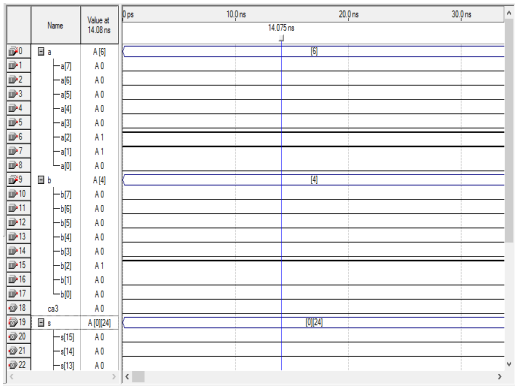

Fig.-7: Simulation result of BEC Based RCA CSLA Multiplier

III. PROPOSED MULTIPLIER ARCHITECTURES

A. Parallel Prefix Adder

The parallel prefix adders [1] are more flexible and are used to speed up the binary additions. Parallel prefix adder architecture [2] is obtained from Carry Look Ahead (CLA) structure. In order to increase the speed of arithmetic operation tree like structure is used [3]. Parallel prefix adders are a group of fastest adders and these are used for high performance of arithmetic circuits in industries. Parallel prefix adders composes of three stages [4] involves three stages

1. Pre-Processing Stage
2. Carry Generation Network
3. Post-Processing Stage

1) Pre-processing stage: In this stage, generate and propagate signals are computed to each pair of inputs A and B. These signals are represented by the logic equations 1 and 2.

Pi=Ai xor Bi (1)
Gi=Ai and Bi (2)

2) Carry generation network: This stage computes the carries corresponding to each bit. Execution of these operations is carried out in parallel [4]. After the carries in parallel are computed, they are segmented into smaller pieces. Carry propagate and generate are used as intermediate signals which are represented by the logic equations 3 and 4.

CPi:j=Pi:k+1 and Pk:j (3)
CGi:j=Gi:k+1or (Pi:k+1 and Gk:j (4)

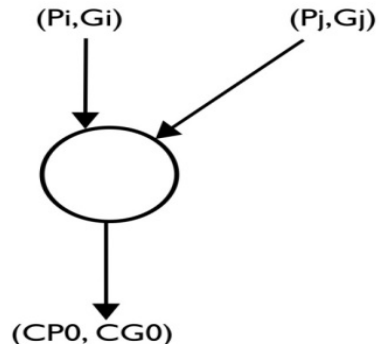

Fig.-8: Carry Network

The operations involved in Fig.8 are given as:

CP0=Pi and Pj (5)
CG0= (Pi and Gj) or Gi (6)

3) Post processing stage: This is the final step to compute the summation of input bits. It is common for all adders and the sum bits are represented by logic equations 7&8.

Ci-1=(Pi and Cin) or Gi (7)
Si=Pi xor Ci-1 (8)

A. Brent -Kung Adder

Brent- Kung adder [5] is a very well- known logarithmic adder architecture giving an optimal number of stages from input to all outputs but with asymmetric loading on all intermediate stages. It is one of the parallel prefix adders. Parallel prefix adders are a unique class of adders that are based on the use of generate and propagate signals. The cost and wiring complexity is less in Brent-Kung adders. But the gate level depth of Brent Kung adders is [6] 0 (log2 (n)), so the speed is lower. The block diagram of 4-bit Brent Kung adder is shown in Fig.9.

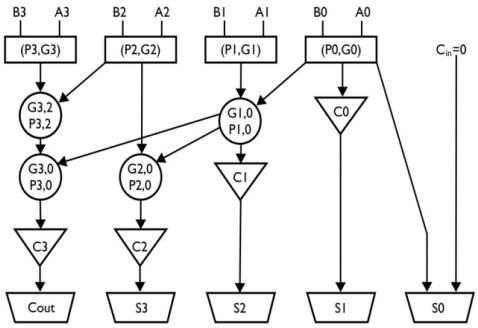

Fig.-9: Block Diagram of Brent Kung Adder

B. Multiplier Using Brent-Kung Adder based Carry Select Adder

Brent-Kung Adder [7] has reduced delay when compared to Ripple Carry Adder. So Brent-Kung Adder based CSLA is designed just by using Brent-Kung Adder. Here the Ripple Carry Adders are replaced by Brent-Kung adder so that delay is reduced. Fig.10. shows the block diagram of 8-bit Brent- Kung based CSLA.

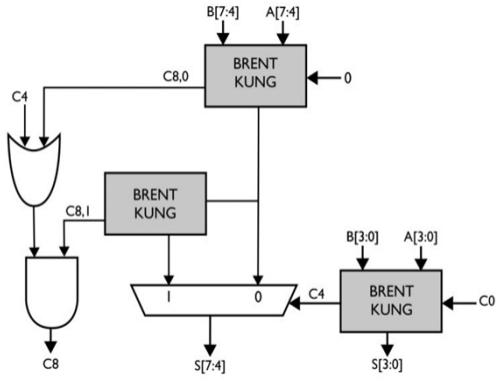

Fig.-10: 8-bit Brent-Kung Adder based CSLA

Thus the 8 bit multiplier uses the Brent Kung adder for the intermediate addition and final addition. Thus as the Brent Kung Adder based CSLA has reduced delay, the multiplier using BK CSLA also has improved speed. Fig.11 shows the block diagram of 8-bit Brent-Kung based CSLA Multiplier. Fig.12 shows the simulation result of 8-bit Brent-Kung based CSLA Multiplier.

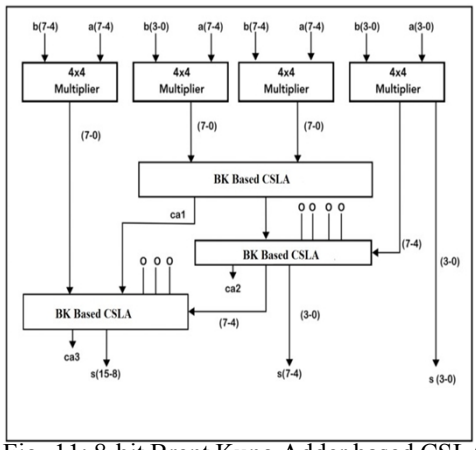

Fig.-11: 8-bit Brent Kung Adder based CSLA Multiplier

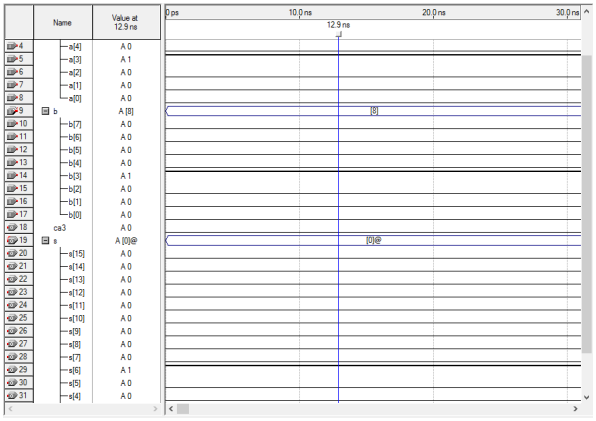

Fig.-12: Simulation result of 8-bit Brent Kung Adder based CSLA Multiplier

IV. SIMULATION RESULTS AND COMPARISON

Various adders and multipliers were designed in Quartus II software. Area and delay of various multipliers like 8-bit Ripple Carry adder based CSLA Multiplier, 8-bit Binary to Excess-1 based CSLA Multiplier and 8-bit Brent-Kung based CSLA Multiplier has been calculated. Table. I shows the comparison of delay in different types of multiplier.

TABLE - I: COMPARISON OF DELAY IN DIFFERENT MULTIPLIERS

TYPE OF MULTIPLIER	RCA Based CSLA Multiplier	BEC Based RCA CSLA Multiplier	BK Based CSLA Multiplier
DELAY	55.200ns	50.200ns	45.400ns

The result analysis shows that 8-bit BK based CSLA Multiplier has reduced delay than all other multiplier architectures with a compromise of area. The graphical representation of comparison of delay of different multipliers is shown in Fig.13. It is evident that BK based CSLA Multiplier has reduced delay than all other multipliers.

The graphical representation of comparison of no. of transistors in different multipliers is shown in Fig.14. Table-2 shows the comparison of no. of transistors in different types of multipliers. It is evident that BK based CSLA Multiplier has increased transistor count than all other multipliers

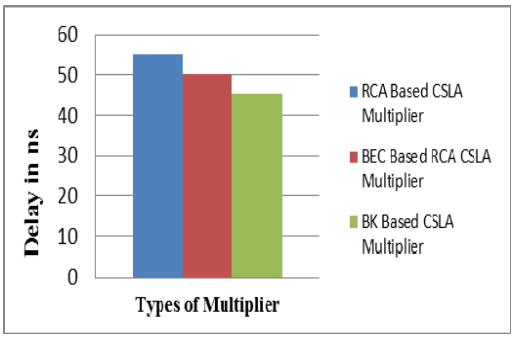

Fig.13.Comparison of delay in different multipliers

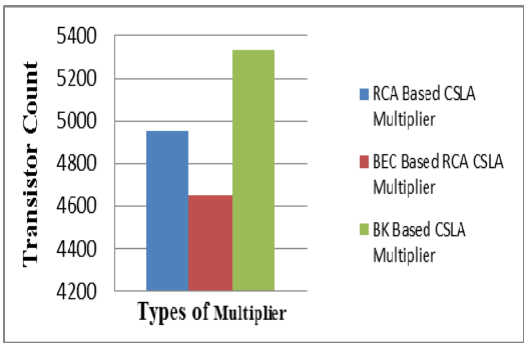

Fig.14. Comparison of no of transistors in different multipliers

Table- 2: comparison of transistor count in different multipliers

UNITS	RCA Based CSLA Multiplier		BEC Based RCA CSLA Multiplier		BK Based CSL Multiplie	
RCA	9	1368	6	912	-	-
MUX	3	222	3	222	3	222
OR	3	18	3	18	3	18
AND	3	18	3	18	3	18
BEC	-	-	3	150	-	-
BK	-	-	-	-	9	1746
4bMULT	4	3328	4	3328	4	3328
TOTAL	22	4954	22	4648	22	5332

V. CONCLUSION

The various adders and multipliers were simulated using Quartus II software and the results show that RCA Based CSLA Multiplier has delay of 55.200 ns, BEC Based RCA CSLA Multiplier has

50.200 ns, BK Based CSLA Multiplier has 45.400 ns. Thus BK based CSLA Multiplier is found to have reduced delay by 17.75 % compared to RCA Based CSLA Multiplier, 9.56% compared to BEC Based RCA CSLA Multiplier. The no. of transistors in RCA Based CSLA Multiplier is 4954, BEC Based RCA CSLA Multiplier is 4648, BK Based CSLA Multiplier is 5332. Thus BK based CSLA Multiplier has improved speed compared to other multipliers with a small compromise in transistor count.

VI.LIMITATION

VII. BK based CSLA Multiplier has reduced delay compared to all other multipliers but the only limitation is that the area is slightly increased due to increased number of transistor count. Thus BK based CSLA Multiplier has improved speed compared to the other multipliers with a small compromise in transistor count.

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