COMPENSATION OF VOLTAGE SAG USING LEVEL SHIFTED CARRIER PULSE WIDTH MODULATED ASYMMETRIC CASCADED MLI BASED DVR SYSTEM

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ABSTRACT

The Dynamic Voltage Restorer (DVR) is a custom power electronic device that is used to inject voltage in series and in synchronism with the distribution feeder voltages in order to compensate for voltage sag/swell. In this paper, a MLI based DVR using Multi carrier pulse width modulation technique is being proposed for compensation of sag/swell in distribution system. Using level shifted carrier pulse width modulated asymmetric cascaded MLI based DVR instead of H-bridge based DVR, the quality of the injected voltage gets improved and the filler size gets reduced. Proposed model is simulated in MATLAB-Simulink and simulation results prove that the proposed model is the most effective solution for the problem of voltage sag/swell.

Keywords: Power quality, Dynamic voltage Restorer [DVR], Cascaded Multilevel Inverter [CMLI], Multi Carrier Pulse width modulation [MC-PWM].

I. INTRODUCTION

A common characteristic of most electronics is that they are sensitive to voltage variations. Voltage variations can be classified as disturbances that produce voltages below the nominal value, which are called voltage sags, and disturbances that produce voltages above the nominal value, which are called voltage swells. Voltage sag is defined as a sudden reduction of supply voltage down 90% to 10% of nominal, followed by a recovery after a short period of time. Atypical duration of sag is 10ms to 1 minute³. Voltage sag can cause loss of production in automated processes since voltage sag can trip a motor or cause its controller to malfunction. Voltage swell is defined as sudden increasing of supply voltage up 110% to 180% in RMS voltage at the fundamental frequency with duration from 10 ms to 1 minute. Switching off a large inductive load or energizing a large capacitor bank is atypical system event that causes swells. During power disturbances Dynamic Voltage Restorer (DVR) installed in front of a critical load will appropriately provide correction to that load only. The voltage sag magnitude depends on various factors like the type of fault, the location of the fault and the fault impedance. Voltage sag/swell is most important power quality problems challenging the utility industry can be compensated and power is injected into the distribution system. By injecting voltage with a phase advance with respect to the sustained source-side voltage, reactive power can be utilized to help voltage restoration. The modeling and simulation of Cascaded MLI based DVR is presented. To reduce harmonics in the MLI multilevel PWM techniques are used. Simulation of MLI based DVR is presented. In this paper the modeling and implementation of Multilevel inverter based dynamic voltage restorer for voltage sag compensation is presented. The simulation results are presented to show the effectiveness of the proposed control method.

II. DESCRIPTION OF THE SYSTEM

Dynamic Voltage Restorer is a series connected power electronic device which injects missing voltage into the system to regulate voltage at the load end in case of any power quality issues like voltage sag or swell in the system. The basic operation of DVR in power system is shown in Fig 1. The main principle behind working of DVR is that it injects dynamically controlled voltage \( V_{ds} \) generated by forced commutated converter in series to the bus voltage by means of a booster transformer. There are different methodologies available for operating DVR which mainly differs in triggering the pulses for the inverter circuit⁶.

Fig. 1. Structure of power system with DVR

There are three different modes of operation of DVR namely protection mode, standby mode and injection mode. The structure of DVR is shown in Fig. 2. The DVR has four components such as energy storage devices, PWM inverter unit, Filter circuit, Injection transformer. In the conventional DVR system, H-bridge inverter based DVR is used⁵.

Fig. 2. Structure of cascaded MLI based DVR in distribution system

In this DVR structure, the PWM inverter is replaced by the cascaded MLI. Hence it improves the quality of the injected voltage. Further reducing the harmonics the Multi-carrier PWM technique is used for triggering the pulses of inverter circuit and it
reduces the THD in the injected voltage. Thus improves the quality of the voltage. In this paper the modeling and implementation of Multilevel inverter based dynamic voltage restorer for voltage sag compensation is presented. The simulation results are presented to show the effectiveness of the proposed control method.

III. VOLTAGE SAG COMPENSATION SYSTEM BY USING H-BRIDGE INVERTER BASED DVR SYSTEM

In order to meet the requirement of constant voltage control, closed loop control operation is performed for the desired value of the voltage according to need. The simulink model of closed loop control of voltage sag compensation in a DVR is shown in Fig. 3. Initially the system was subjected to 15% voltage sag at t=0.3s and remains up to t=0.7s with the total voltage sag duration of 400ns, in a run time of 1s.

Fig. 3. Simulink model of single phase powersystem with DVR using H-bridge inverter

The subsystem 1 contains rectifier and PI controller shown in fig 4. The signal from the controller is given to subsystem 2, the subsystem 2 contains H bridge inverter which is being controlled by PI controller shown in fig. 5.

Fig. 4. Simulink model of DVR subsystem 1

Fig. 5. Simulink model of DVR subsystem 2

IV. VOLTAGE SAG COMPENSATION SYSTEM BY USING CASCADED MLI BASED DVR SYSTEM

In order to meet the requirement of constant voltage control, closed loop control operation is performed for the desired value of the voltage according to need. The Simulink model of closed loop control of voltage sag compensation in a DVR, is shown in Fig. 9. Initially the system was subjected to 15% voltage sag at t=0.3s and remains up to t=0.7s with the total voltage sag duration of 0.4s, in a run time of 1s.

Fig. 6 shows the input AC voltage with 15% sag from the period 0.3s to 0.7s.

Fig. 6. Output voltage waveform with voltage sag

Fig. 7 shows the DVR injected voltage from the H-bridge based DVR. The injected voltage is in phase with the supply voltage and gets added up thus the voltage sag is compensated and is shown in fig. 7.

Fig. 7. Injected voltage

In this H-bridge inverter based DVR system the quality of the injected voltage is not good. Hence filter is needed to improve the quality of the injected voltage.

Fig. 8. Compensated voltage waveform
Fig. 9. Simulink model of single phase power system with DVR using asymmetric cascaded MLI based DVR

![Simulink model of single phase power system with DVR using asymmetric cascaded MLI based DVR](image)

Fig. 10. Simulink model of DVR subsystem 1

The subsystem 1 contains the bridge rectifier and a PI controller. Where the control signal from PI controller is given to the cascaded multi level inverter. The subsystem 1 is shown in the Fig. 10. The subsystem 2 contains the cascaded multilevel inverter which injects required voltage into the system. It is shown in the Fig. 11.

![Simulink model of DVR subsystem 1](image)

Fig. 11. Simulink model of DVR subsystem 2

Fig. 12 shows the input AC voltage with 15% sag from the period 0.3s to 0.7s.

![Simulink model of DVR subsystem 1](image)

Fig. 12. Output voltage waveform with voltage sag

Fig. 13. Injected voltage

The injected voltage is in phase with the supply voltage and gets added up thus the voltage sag is compensated and is shown in Fig. 14.

![Simulink model of DVR subsystem 1](image)

Fig. 13. Injected voltage

Fig. 14. Compensated voltage waveform

In this cascaded MLI based DVR the quality of the injected voltage is improved and hence the requirements of the filter circuits get reduced.

1. **CASCADED MULTILEVEL INVERTER**

Cascaded Multilevel Inverter (CMLI) is one of the most important topology in the family of multi-level inverters. It requires least number of components with compare to diode-clamped and flying capacitors.
type multilevel inverters. The CMLI consists of a number of H-bridge inverter units with separate dc source for each unit and is connected in cascade or series as shown in Fig. 14. The ac output of each H-bridge is connected in series such that the synthesized output voltage waveform is the sum of all of the individual H-bridge outputs.

An eleven level symmetric cascaded multi-level inverter consists of five H-bridge cascaded with equal voltage source in single-phase. Where asymmetric cascaded consists of only 3 H-bridge units with voltage ratio of 1:2:2. A multilevel inverter synthesize a desired voltage from several separate dc sources (SDCS’s), which may be obtained from batteries, fuel cells, or solar cells. Each SDCS is connected to a single-phase full-bridge inverter. Each H-bridge can generate three different voltage outputs (+\(V_{dc}\), 0 and \(-V_{dc}\)) by the different combinations of the four switches (\(S_1\), \(S_2\), \(S_3\) and \(S_4\)). Since then, the CMLI has been utilized in a wide range of applications. With its modularity and flexibility, the CMLI shows superiority in high-power applications, especially shunt and series connected FACTS controllers.

![Generalized structure of cascaded multilevel inverter](image)

In the present work, in the carrier-based implementation the phase disposition PWM scheme is used. Fig. 15 demonstrates the in phase disposition reference and carrier schema for a eleven-level inverter. All the carrier signals are in phase. The rules for the in phase disposition method, when the number of level \(N = b\), the \(b-1\) carrier waveforms are arranged so that every carrier waveforms are in phase. Sine wave is the reference signal where frequency is 50Hz. The sine wave cuts the carrier waveforms which generates pulses to the switches.

![Level shifted PWM reference and carrier waveform schema](image)

### ii. simulink model of asymmetric cascaded eleven level inverter

Due to reduction in the number of DC sources employed the structure becomes more reliable and the output voltage has higher resolution due to increased number of steps and the reference sinusoidal can be better achieved. An asymmetric cascaded MLI is shown in the Figure 8. It is used to generate 11 level output for the DC sources in the ratio 1:2:2. By different combinations of 12 switches, \(S_1-S_{12}\), each inverter can generate three different voltage outputs, \(+V_{dc}\), \(-V_{dc}\) and Zero. With the below circuit, it is possible to obtain a maximum of 11level with the ratio 1:1:2. Switching states are developed for positive, negative and zero voltages and with these patterns the switching table is developed and the gate pulses are generated. The generated pulses are given to each switch in accordance with the Table I and the output is obtained.

![Simulink model of asymmetric cascaded 11-level MLI](image)

### iii. switching sequence

Table I gives switching pattern for a eleven level inverter. The switching table is formed in accordance with the output level and each pulse is generated with that. The asymmetric switching pattern involves a combination of all the H-bridges for each level. Those patterns are perfectly designed such that the circuit gets closed at each level and in that way the switching table is developed for the positive and negative voltage levels.

**TABLE I** switching pattern for asymmetric eleven level MLI.
The obtained output of 11 level cascaded asymmetric multilevel inverter is shown in the Fig. 17.

iv. level shifted PWM based asymmetric eleven level inverter

In MLI, switching pulses are generated and in case of MCPWM level shifting carriers signals are generated. The multicarrier are developed using repeated sequences whose peak for each level is determined. The multicarrier are generated for both positive and negative half cycle and then it is combined using logical operator to produce the corresponding pulses for each switch. Once they are combined they are given to the corresponding switches and the output is obtained for multicarrier PWM for eleven level inverter.

The subsystem is shown in Fig. 19. The modulation strategy employed in the circuit is In Phase Disposition (IPD). An n-level inverter using level shifted MCPWM requires n-1 triangular carriers, all having same frequency and peak to peak amplitude, hence for 11 level inverter, 10 no. of carriers are used. The frequency modulation index \( m_f \) remains same and is defined as given in equation 1.

\[
m_f = \frac{f_c}{f_s}
\]  

(1)

The amplitude modulation index \( m_a \) is defined as shown in equation 2.

\[
m_a = \frac{V_m}{V_{cr}(n-1)}
\]  

(2)

The subsystem of the main circuit are shown in Fig. 19. The subsystem is used for generation of multi carriers for positive and negative half of the generated waveform. The multi carriers are generated first and are compared with a sine wave for first half cycle. Then patterns are generated for the instance at which sine PWM should be introduced for each switches. The generated signal constitute only for the positive half cycle. The same procedure is repeated for the negative half cycle and a separate subsystem is created for the negative half. Now, for both the PWM for each switch is combined with the help of a logical operator and given to the respective switches.

The modulated output for the multi carrier PWM based 11 level inverter is shown in Fig 20. The eleven level shifted PWM inverter output voltage is shown in the Fig 20.
The FFT analysis is performed to calculate the THD of the obtained modulated output. The FFT spectrum of output voltage waveform of level shifted PWM eleven level inverter is shown in Fig. 15.

v. FFT spectrum and analysis

The FFT analysis is performed to calculate the THD of the obtained output of single H-bridge inverter. The FFT spectrum of single H-bridge inverter is shown in Fig. 21. Hence the requirement of filter is high to improve the quality of the injected voltage.

The FFT spectrum of output voltage waveform of level shifted PWM eleven level inverter is shown in Fig. 23.

From the above analysis, it is very clear that there is a drastic change in THD of the output after modulation has been performed. The THD has been reduced to 11.03%.

<table>
<thead>
<tr>
<th>TYPE</th>
<th>THD (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Eleven level MLI</td>
<td>21.15</td>
</tr>
<tr>
<td>Level shifted eleven level MLI</td>
<td>11.03</td>
</tr>
</tbody>
</table>

Table III gives the comparison of THD level between single H-bridge inverter and MCPWM based asymmetric eleven level MLI. Hence it is cleared that the injected voltage from asymmetric cascaded MLI based DVR is better than the single H-bridge inverter.

v. CONCLUSION

The implementation of MLI based DVR system using PI controller has been presented. DVR is an effective custom power device for voltage sag mitigation. The impact of voltage sag/swell on sensitive equipment is severe. Therefore, DVR is considered to be an efficient solution due to its low cost, small size and fast response. Hence using the cascaded MLI based DVR instead of H-bridge inverter based DVR the quality of the injected voltage gets improved and it’s reduced the filter size. The simulation results indicate that the implemented control strategy compensates for voltage sags/swells with high accuracy. The results show that the control technique is simple and
efficient method for voltage sag compensation and the quality of the injected voltage is improved and the filter size gets reduced.

REFERENCES


