Analysis of the effect of NBTI on data flip time dependency on an MTCMOS SRAM

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ABSTRACT

The predominant restraining factor of the circuits lifespan are Temperature Instability effects like NBTI and PBTI. A regular configuration to evaluate the influence of NBTI on a circuit's operation is developed relating significant circuit constraints such as the node switching action, variation in supply voltage, temperature etc. The influence of NBTI on Read strength of SRAM cell is analyzed. Due to the NBTI stress, the working of the SRAM is totally affected. The consignment of deterioration in Static Noise Margin (SNM), is computed by the read steadiness of SRAM cells is appraised. We suggest a novel method to retrieve the SNM of SRAM cells employing a data flip process and portray the results obtained. The performance issues of the data flip time are analyzed by HSPICE simulation with varied supply voltages. The circuit design with NBTI stress is calculated depends upon the simulation setup of HSPICE tool. The supply voltage is varied by 0 V, 0.2 V, 0.4 V, 0.6 V, 0.8 V and 1 V with a length of 45nm and width of 90nm (Taken from PTM technology).

Index terms: Static Noise Margin, NBTI, PBTI, Data flip dependency

I. INTRODUCTION TO NBTI

The tremendous scaling of CMOS technologies over-time has raised modern reliability issues, like BIAS Bias Temperature Instability in PMOS devices. (NBTI). NBTI profoundly deteriorates PMOS transistors and could achieve up to 50mV variations in V_{th} during a timeframe of few years, transferring to greater than 20% deprivation in circuit's speed or under worst scenarios leading to functional failures. Tentative data suggests that NBTI exacerbates exponentially using thin gate oxides and high operational temperatures (T). As the gate oxides become than 4nm, NBTI will circumspectly turn into the limiting factor of circuits life expectancy [6]. Hence, it is crucial to design techniques to perceive, test, and recover from the deterioration of circuits interpretation in the existence of NBTI, to guarantee reliable circuits functionality in a desired lifetime. The investigation of NBTI is a very complex than that of classical reliability concerns like hot-carrier effects, because NBTI shows stress and recovery phenomenon in dynamic working. Based on the duty cycles and input pattern, approximately 75% of former NBTI-induced deterioration is recovered by applying to the PMOS gate a voltage (V_{dd}). An accurate presumption of degradation in performance shall involve V_{dd}, T, the switching action of a node. These constraints are not temporally constant, but transform profoundly from gates to gates and from timeframes reflecting the un-certainty in circuit topology and functionality. These irregularities must be integrated in analysis of degradation for short and long-term evaluations. Simple static analysis can contribute in extremely worst estimation cases.

II. DESIGN APPROACHES FOR NBTI MODELING

The performance degradation of circuits resulting due to NBTI effects is perceptive to node actions, Temperature. Hence, design practices during the premature design stages are applied to mitigate NBTI effects. The design practices include**:**

(1) **Optimize node activities:** For the circuits in stand-by phase, a designated sets of input vectors to logic cells or memories are chosen to maximize the recovery from NBTI effects. For circuits operating in active phases, the inputs signal α is chosen to make the comparative time it stays in nonoperating mode for a lengthy duration. The experimental results portray that the optimizations shall achieve 2-4X minimization of delay deprivation resulting due to NBTI.

(2) **Adjusting the supply voltages:** Although less V_{dd} is desired for reducing the quantity of NBTI effects, this analysis for intuitively deterioration obtained due to NBTI effects doesn't hold valid. In contrast, low operating supply voltages may result in severe degradation for higher voltage for 65nm.

Selection of optimal operating V_{dd} for NBTI effects elimination must be made. The perfect optimized operating V_{dd} value reckons on the processes, environmental conditions, inputs signals probabilities, etc.

(3) **Decrease in Temperature.** Minimizing temperatures is a very good method to recuperate from Natator experiments prove that reducing the IC temperature might result in up to 60% decrease in the delays.

(4**) Resizing**. Circuits delay depends on the sizes of the transistor devices, increase in the size of the transistors is one way to suppress gate delay. Resizing the paths which are sensitive to NBTI effect can reduce the effect of the path delay rise arising owing to NBTI on the entire circuit. However, it will increase the area cost, reference has demonstrated that delay degradation due to NBTI effect can be offset using gate sizing (8.7% average circuit size increase.

III. MTCMOS LOGIC

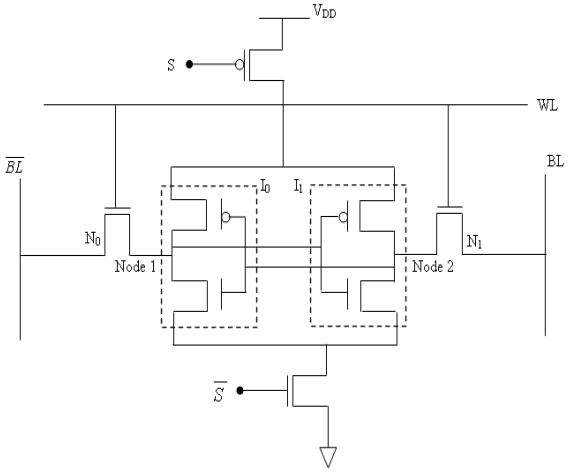

Fig 1: 6T SRAM using MTCMOS Logic

Low-power architectures are employed ranging from the process levels to algorithmic levels. Menacing the supply voltage (VDD) is one that notably curtails the power dissipation due to orthogonal relationship amidst the supply voltage and the switching power dissipation [19]. To indemnify for the deprivement in-functionality due to a low supply voltage, a device threshold voltage (V_{th}) shall be restricted. Despite, this results in a rise in the sub-threshold leakage currents. Hence the, prominent area today is to design circuit approaches to mitigate the sub threshold leakage currents induced by reduced V_{th}. Multi Threshold Complementary Metal Oxide Semiconductor (MTCMOS) is an emergent Circuit-level method providing a high attainment and less leakage powers scenario. However, the techniques employ devices in the standby phase to segregate the power supplies. As an outcome, the speed of the circuit in the active phase degrades owing to the presence of sleep transistors.

The modification is sleep transistors s1 and s2, the operation of SRAM based on these sleeping transistors only. If s1=0 and s2=1, both sleeping transistors s1, s2 are ON and the circuit will be in active mode otherwise circuit goes to sleeping mode. The operation of the modified structure of SRAM cell. The simulation is performed using the Cadence ORCAD simulator for a 32-nm process using the Predictive Technology Model. Recovery boosting can be achieved by two techniques one is fine granularity, such as for single entries/rows of a memory array, or at a coarse granularity, for an entire array.

IV. MTCMOS SRAM FOR FINE GRAINED RECOVERY BOOSTING: In table III, sleep transistor input s is 0 (i.e. active mode or normal mode), the states of the bit lines change during read and writes functions. Owing to a pair of bit lines being shared by all the Memory cells in each column in the array, even the memory cells not being read from or written to shall have voltages on the bit lines modified. In an ordinary RAM array, these bit line transitions won't affect the normal operation of the cells. But, to perform recovery boosting of a memory cell, both bit lines of the cell need to be raised toV_{dd}. So, we need able to isolate the bitlines of the memory cells that are in the recovery boost mode from the bitlines that are used for accessing other cells in the array. To make this modification extend the memory cells having connections to rails of an adjoint row or columns through two pMOS access devices. The design of Fine-grained Recovery boosting in SRAM cells is shown below.CR =1 the cell goes to recovery boost mode, moreover raise the ground voltage to 1, two extra pMOS devices are also turned on. With these connections, we can put the cell in to recovery mode individually. These devices do not affect performance strongly but and faster way achieve the mode transition (i.e. transition between the normal mode to recovery boost mode), but the architecture required more area.

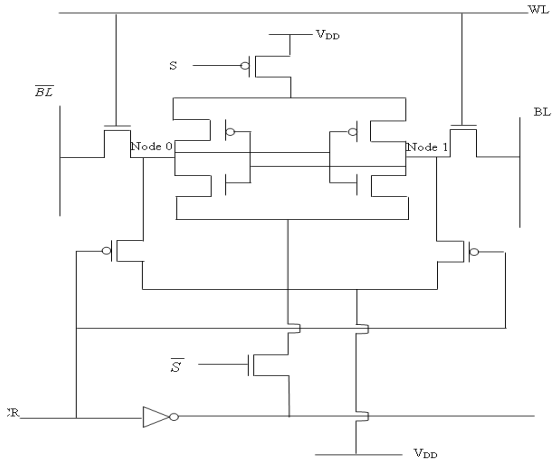

Fig. 2: Fine Grained Recovery Boosting in 6T SRAM with MTCOS

V. RESULTS AND DISCUSSION

5.1: Data-flip Time Dependency on NBTI: Due to the NBTI stress, the performance of the SRAM cell is totally affected. The performance issues of this problem is analyzed by HSPICE simulation with different supply voltages. The circuit design with NBTI stress is calculated depends upon the simulation setup of HSPICE tool. The supply voltage is varying by 0V, 0.2V, 0.4V, 0.6V, 0.8V and 1V with the length of 45nm and width of 90nm (Taken from PTM technology). The Monte-Carlo simulation is shown below.

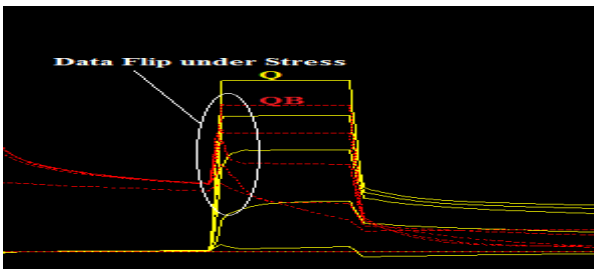

Fig. 3: Monte-Carlo simulation of SRAM read operation with Data flipping

The SRAM cells possesses positive sensing windows, read functions can be performed effectively by employing careful word line and Sense amplifier controls. Another way to express the NBTI stress is by Signal to Noise Margin of the SRAM cells with the supply voltage of 0.6mV. To follow the setup on 6T conventional SRAM cell, if write line is low then the result is hold previous value of the stored memory otherwise perform read and write operation. In read operation, output nodes will observe what present on bit and bit bar line. To write '1' means, to apply '1' into bit line and '0' into bit line bar then the output node of 1,2 is 0,1 respectively; to write '0' means, apply '0' into bit line and '1' into bit line bar then the output node of 1,2 is 1,0 respectively. Another way to express the NBTI stress by Signal to Noise Margin of the SRAM cell i.e. is shown in fig. 10 with the supply voltage of 0.6mV.

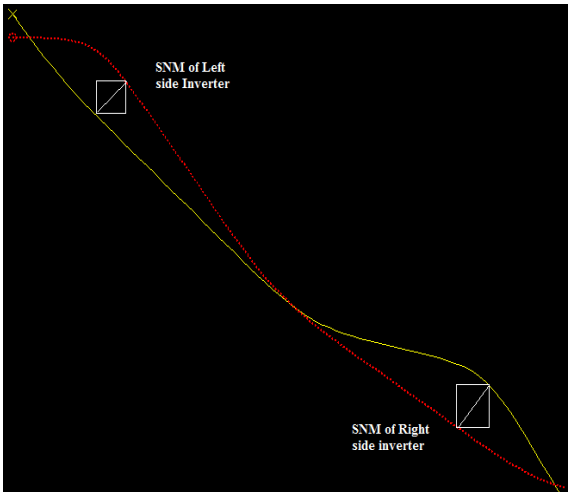

Fig.4: SNM calculation for the SRAM

Depending on the VTCs, the Read margins are characterized by the SRAM cell Read stability. The read margin depends on the transistor's current description. Results indicate that the read margin precisely evaluates the SRAM's Read stability as an act of the threshold voltage modifications and the power supply fluctuations. Results show that the read margin of an SRAM cell during read operation is directly proportionate to cells ratio. Read margins buildups with the elevation in the pull up ratio. Design of SRAM cell inverters is to be done with care for validating the read margins of SRAM cells in read operations. Pull-up ratio hinges on the dimensions of the devices. The technique of analysis of Read margins is similar to the evaluation of static noise margin and the SNM estimations.

SNM = length of the diagonal of square (L) / √2 ⟶

From the SNM simulation, to calculate the length of diagonal of square (L) and the value of each side length is determined. The SNM of simulated design is 220mV at the supply voltage of 0.6V. If the SNM of SRAM cells results in a null value or negative, data-flips occur amidst the disturbing current in the bit lines upto cell nodes. If SNM results in a much negative value, the speeds at which data-flips occur is fast. This results since the more negative the SNM, it delivers higher voltage disruptions in the cell nodes and positive feedback of the cross-coupled inverters amplifies it vastly.

TABLE 4: The Impact Of NBTI On Time To Data-Flip

Threshold voltage degradation (mV)	Time to data flip (μS) depends upon the Supply voltage (VDD)				
	0.2V	0.4V	0.6V	0.8V	1V
50	15.4	17.1	17.5	17.7	17.8
100	14.9	15.3	15.8	16.9	17
150	14.1	14.8	15.1	15.7	16.5
200	13.5	13.6	14.2	14	15.4
250	12.1	12.7	13.5	13.9	14

5.2: Fine Grained Recovery Boosting in 6T MTCMOS SRAM for mitigating NBTI effect

Sleep transistors input s is 0 (i.e. active mode or normal mode), the states of the bit lines changes in read and writes modes. A a pair of bit lines is common to all the memory cells in a specific column in an array, even the memory cells not being read from or written to shall have the voltage on the bit lines modified. In normal SRAM arrays, these bit lines transition doesn't disturb the normal functionality of the cells. For recovery boosting of a memory cell, the 2bit lines of the cells have to be applied toV_{dd}. So, we have to segregate the bit lines of the memory cells in the recovery boosting mode from the bit lines being used for using other cells in an array. To make the modification stretch out the memory cell with connections to the rail of a nearby row or a column through two pMOS devices and the simulation are performed with different supply voltage and is shown in fig. 11. From this simulation result the both inverter outputs Q and QB are not flipped because the recovery boosting method will provide to change states of pMOS transistor from 1 to 0.

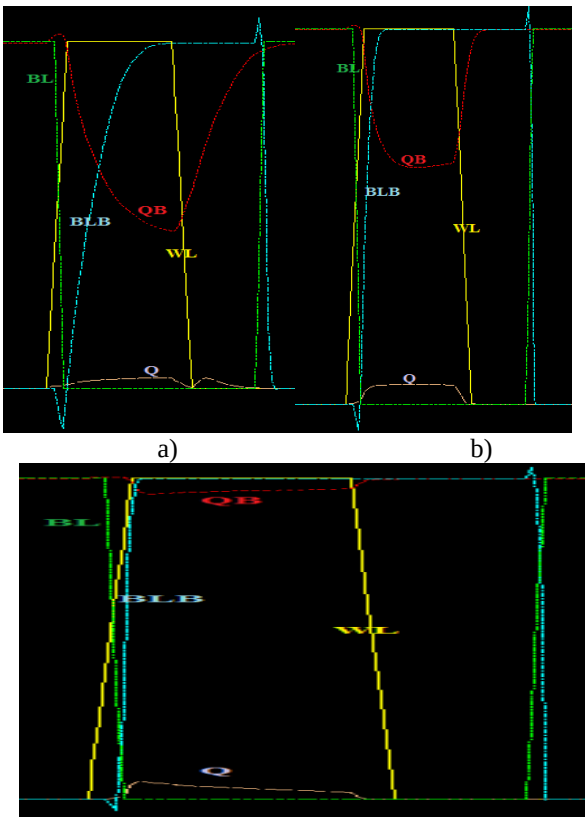

Fig. 5: SRAM read operation without data flipping based on recovery boosting in 6T MTCMOS SRAM cell (a) at VDD=0.2mV (b) at VDD=0.4mV (c) at VDD=0.6mV

VI. CONCLUSION

A complete NBTI experimental analysis depicting the time to data-flip, the sensing window, and the bit line swings have been presented for the proposed architecture. The simulation results project that all the parameters involving time to data-flips, sensing windows and bit line swings, deteriorate as the amount of the stress is elevated. However, since the SRAM cell has positive sensing windows, read operations can be conducted successfully through a careful word line and sense amplifier controls.

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